



# Q77H2-AD

Rev : 1.0.

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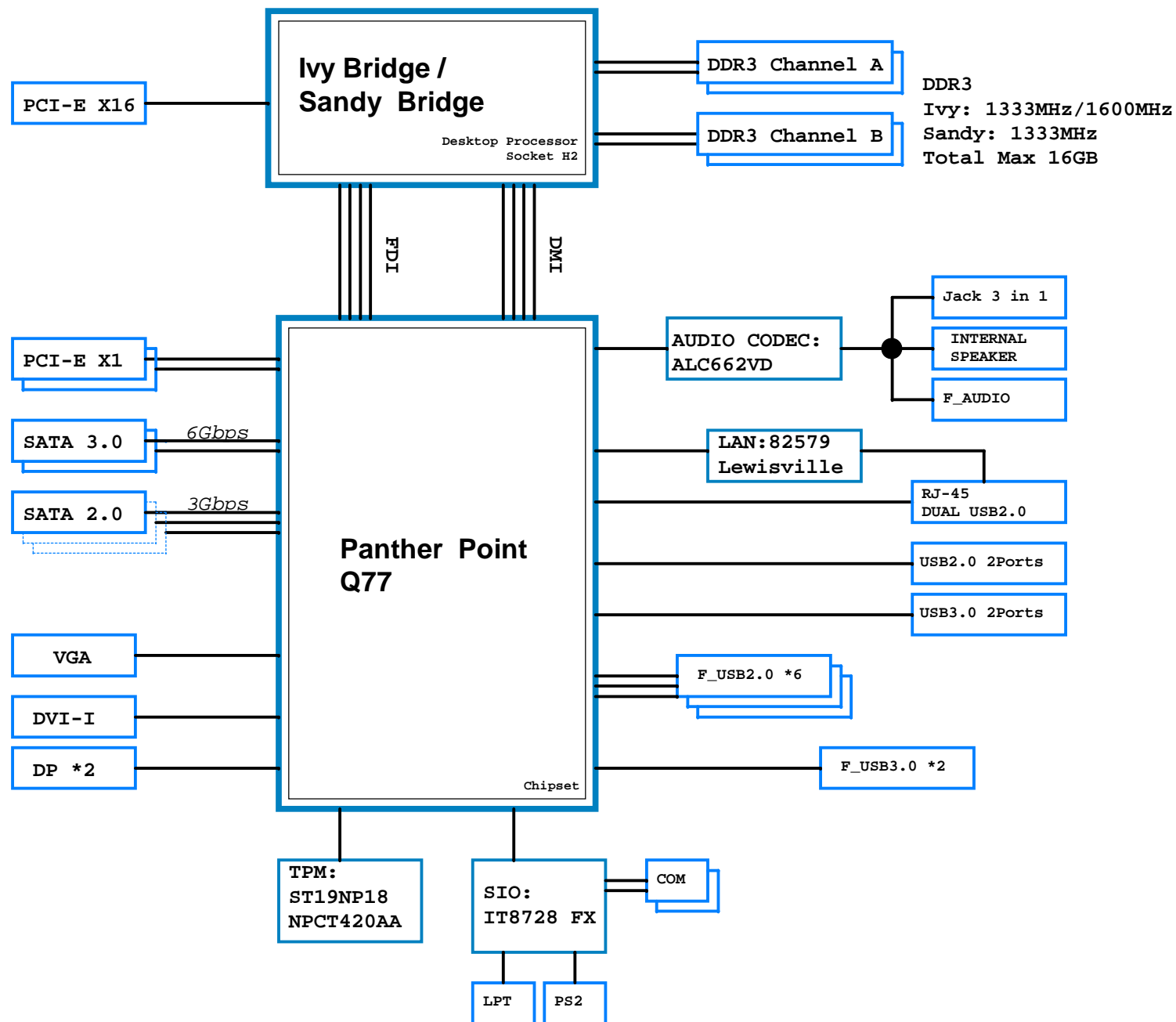
NOTE:

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## REVISION HISTORY:

Rev	Date	Notes
V.A	2011/10/03	Initial version
V.B	2011/12/13	
V1.0	2012/01/17	
V1.0.	2012/04/10	

 <b>Elitegroup Computer Systems</b>		
Title <b>Cover Page</b>		
Size Custom	Document Number <b>Q77H2-AD</b>	Rev <b>1.0.</b>
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## GPIO Table

### PCH

Name	Type	Voltage	Default	Function
GPIO1	I/O	+VCC3	Input	OBR
GPIO6	I/O	+VCC3	Input	Thermal Shut Down
GPIO13	I/O	+3VSB	Input	LPC_PME_L
GPIO15	I/O	+3VSB	Input	TLS_EN
GPIO23	I/O	+VCC3	Input	HDPANEL_DETECT
GPIO27	I/O	SB_3VSB	Input	LANWAKEB for Bcm
GPIO28	I/O	+3VSB	Input	ON_DIE_PLL_EN
GPIO45	I/O	+3VSB	Input	SPL_WPSW
GPIO57	I/O	+3VSB	Input	SPL_WP0_L
GPIO59	I/O	+3VSB	Input	LAN_LED_D
GPIO61	I/O	+3VSB	Input	LPCPD_L
GPIO72	I/O	+3VSB	Input	GPIO72_S4S5

### IT8728F D/EX

Name	Type	Voltage	Int. Res.	Function
GP14	I/O	+VCC3	OD	Thermal Shut Down
GP15	I/O	+VCC3	OD	MB_ID1
GP16	I/O	+VCC3	OD	PC BEEP
GP22	I/O	+3VSB	OD	LED1
GP23	I/O	+3VSB	OD	LED0
GP35	I/O	+VCC3	OD	MB_ID2
GP36	I/O	+VCC3	OD	GPO36 FOR ACER reserve
GP64	I/O	+VCC3	OD	GPO64 FOR ACER reserve

## Straping Table

### PCH Straping (Page.14)

#### TLS Confidentiality:

TLS_EN (internal PD)	
H	Enable TLS
L	Disable TLS

#### No Reboot:

PCH_SPKR (internal PD)	
H	Enable No Reboot
L	Disable

#### On-Die PLL VR:

ON_DIE_PLL_EN (internal PU)	
H	Enable
L	Disable

#### On-Die PLL VR Source:

HDA_SYNC_R (internal PD)	
H	1.5V
L	1.8V

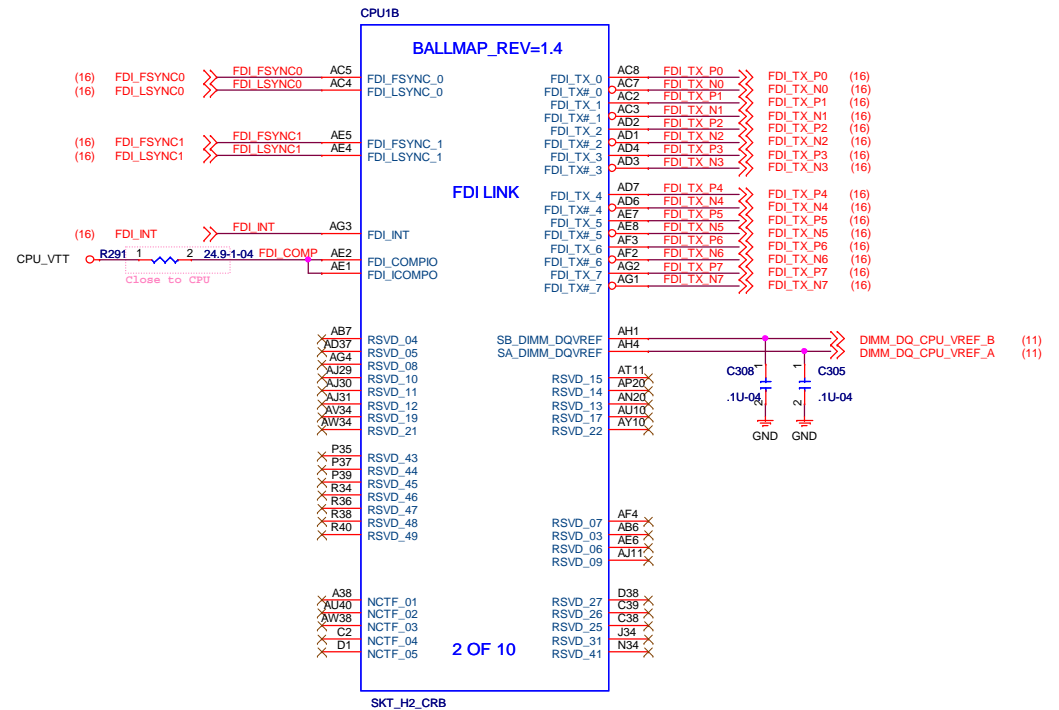
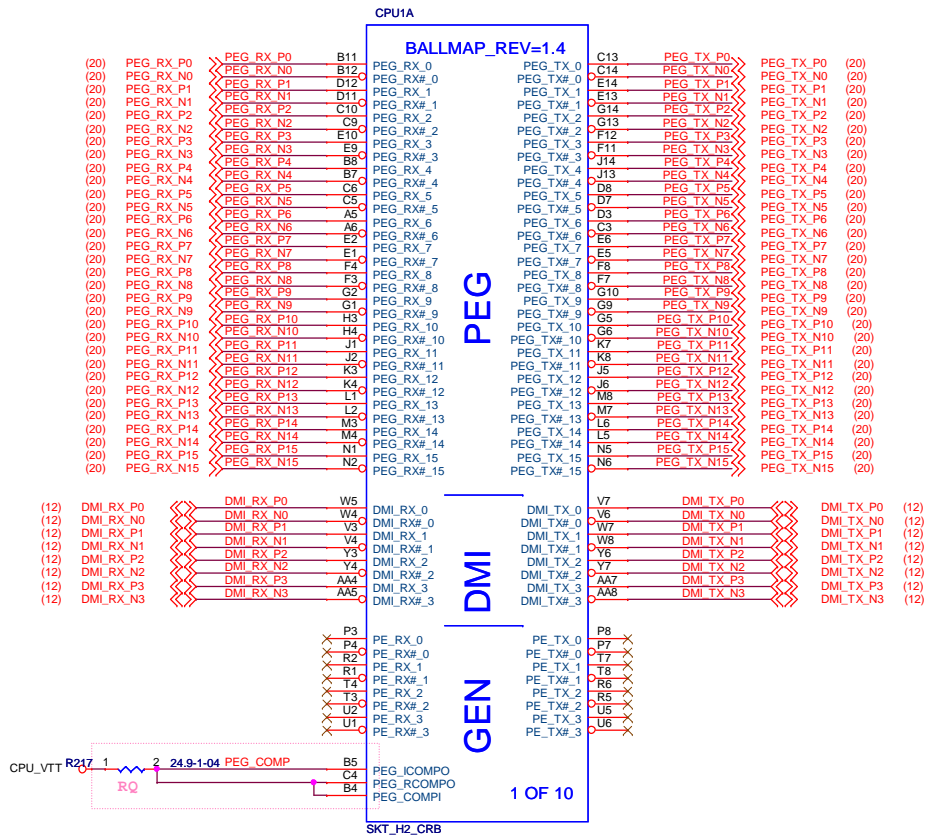
#### Integrated 1.05V SUS VRM:

INTVRMEN	
H	Enable
L	Disable

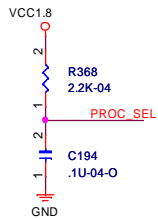
### SIO IT8728F D/EX Straping (Page.28)

#### Power-On Strapping

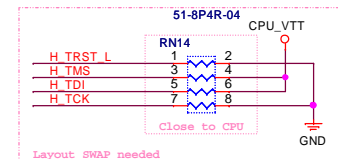
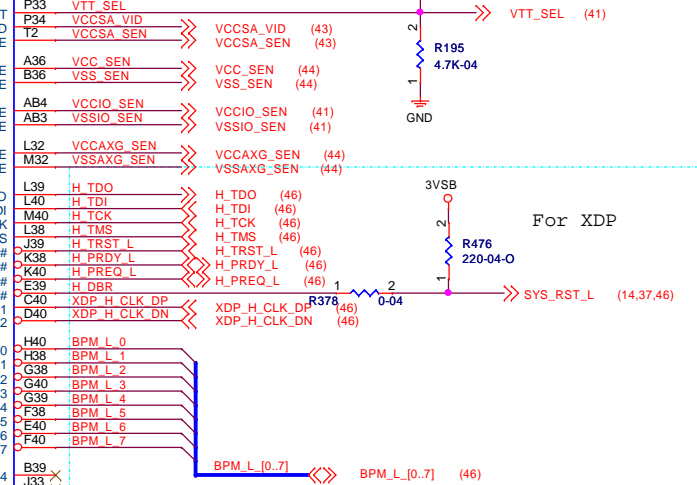
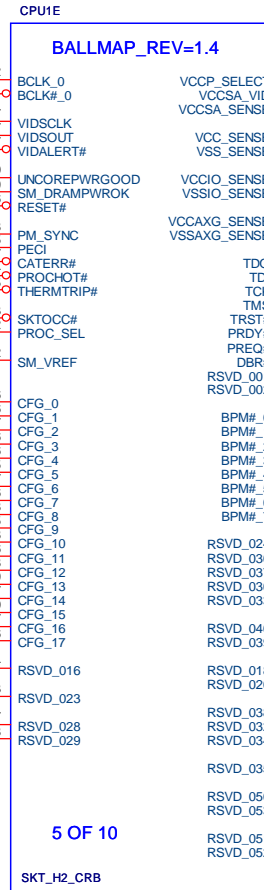
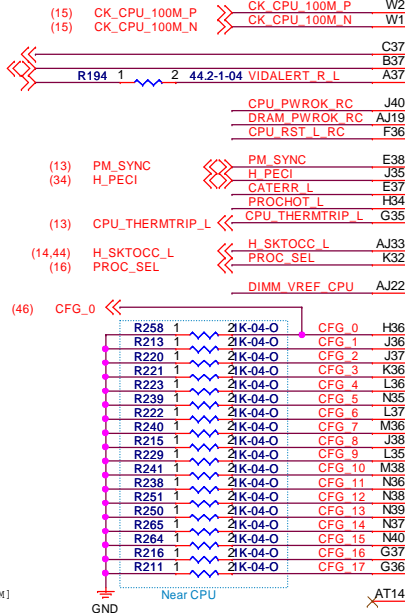
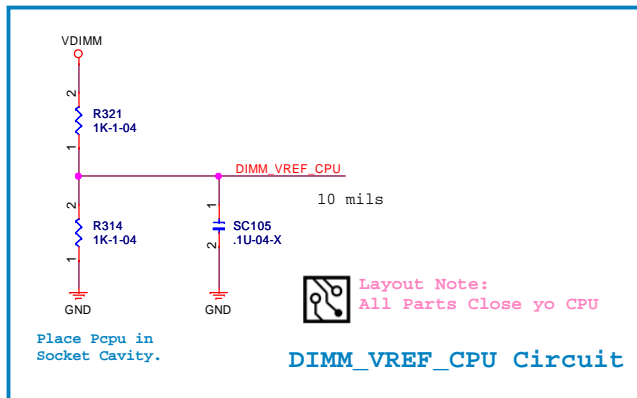
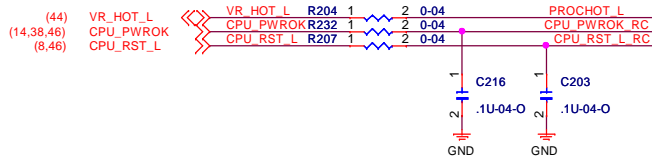
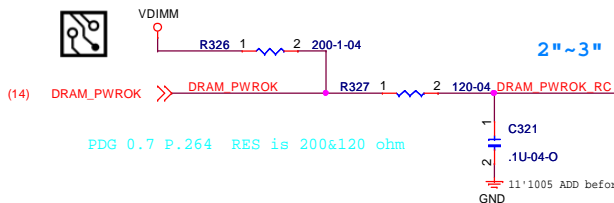
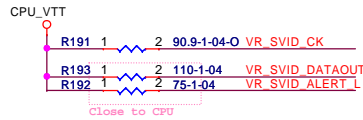
	Symbol	Value	Description
JP1 Pin-48	DSW_EUP_SEL	1	EUP
		0	DSW
JP2 Pin-122	WDT_EN	1	Disable WDT to reset PWROK
		0	Enable WDT to reset PWROK
JP3 Pin-124	FAN_CTL_SEL	1	EC Index 63h/6Bh/73h is 80h
		0	EC Index 63h/6Bh/73h is 00h
JP4 Pin-126	K8PWR_EN	1	Disable K8 Power Sequence
		0	Enable K8 Power Sequence
JP5 Pin-29	UOVMODE_SEL	1	Notice Mode (Default)
	OV/UV	0	Force Mode



SHORT B4 & C4 TOGETHER, ROUTE AS A SINGLE 4MIL TRACE TO RQ.  
 1 ROUTE B5 TO RQ. 1 AS A SEPERATE 12MIL TRACE.



DMI/FDI TERMINATION VOLTAGE  
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH  
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW  
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



CFG	H	L	DESCRIPTION
0	reserved	reserved	reserved
1	reserved	reserved	reserved
2	NORMAL	REVERSE	PEGLANE REVERSAL[0], X16
3	reserved	reserved	reserved
4	reserved	reserved	reserved
5	*	*	PEOFGSEL[0]
6	*	*	PEOFGSEL[1]
7	reserved	reserved	reserved
8	reserved	reserved	reserved
9	reserved	reserved	reserved
10	reserved	reserved	reserved
11	reserved	reserved	reserved
12	reserved	reserved	reserved
13	reserved	reserved	reserved
14	reserved	reserved	reserved
15	reserved	reserved	reserved

PCIE CONFIG	SEL0	SEL1
1 X 16	1	1
2 X 8	0	1

CFG[5:6]:  
11=DEFAULT X16,  
01=2X8,  
10=RESERVED,  
00=X8,X4,X4

**Elitegroup Computer Systems**

Title: **CPU - MISC**

Size: Custom

Document Number: **Q77H2-AD**

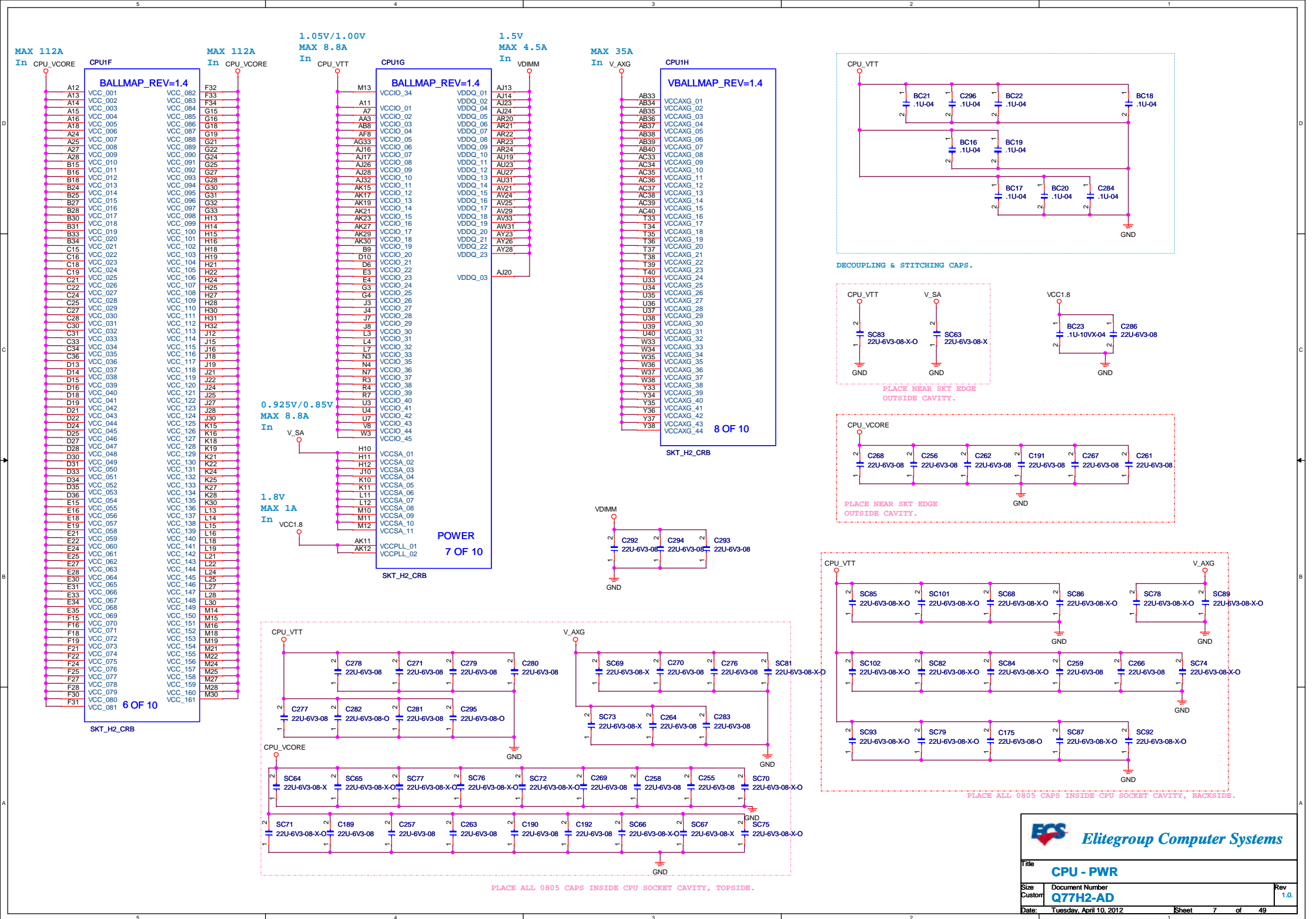
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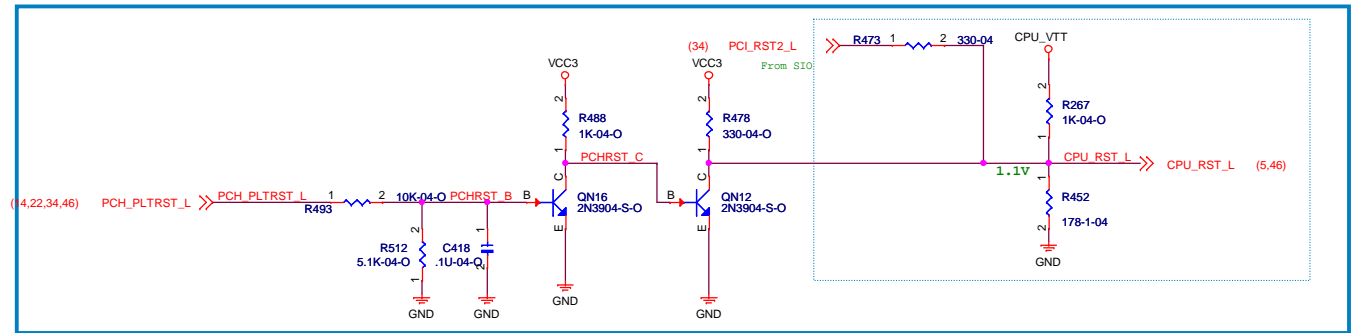
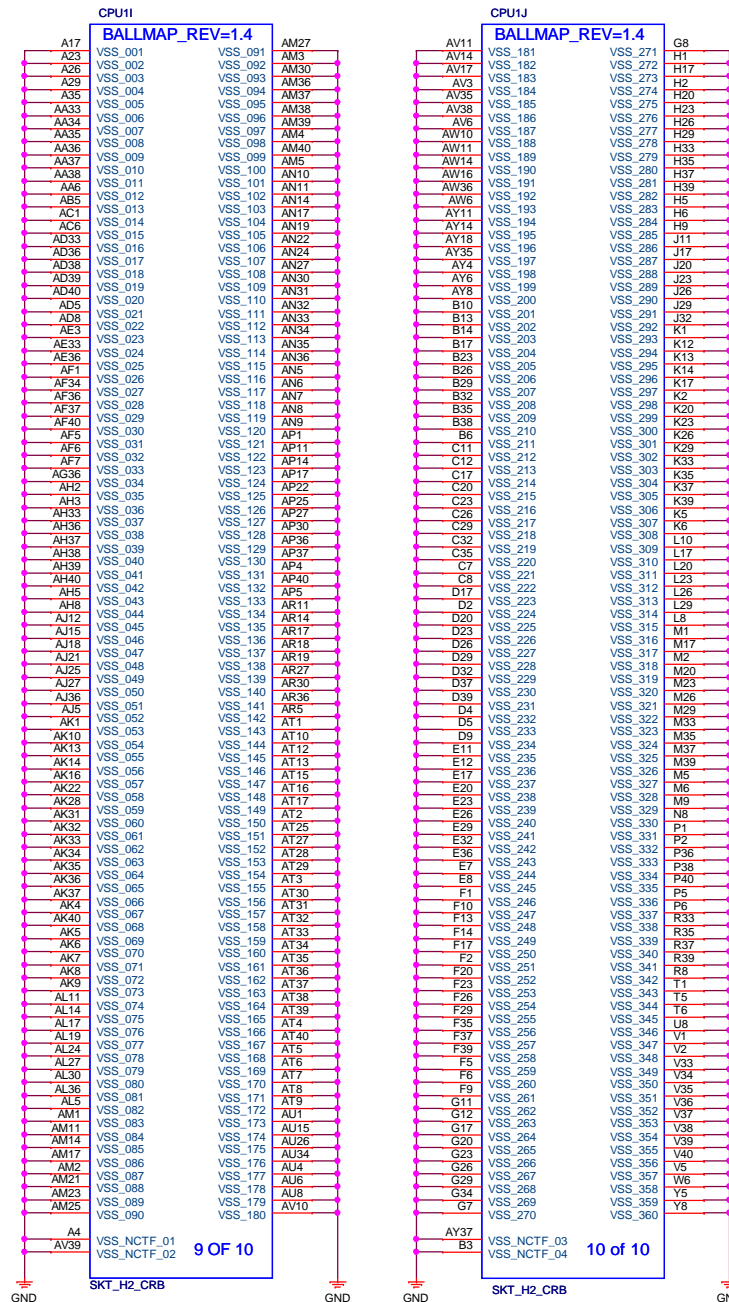
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CFG\_0..17 HAVE INTERNAL PULL-UPS





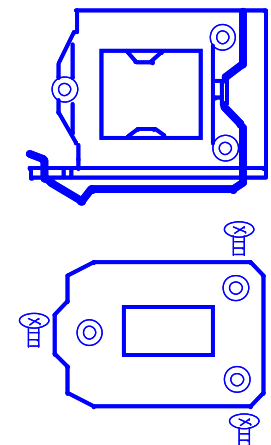




11-018-115123 CPU SMD SOCKET  
SOCKET.CPU.LGA 1155P SMD..G/F...BLACK.  
ACA-ZIF-096-E02....LEAD-FREE(RoHS/HF).L0TES

20-800-005011 SUBASSY.STEEL....LGA 1155P.....  
W/BACK PLATE.ACA-ZIF-082-E23....LEAD-FREE(RoHS).L0TES

CPU(104)  
CPU\_SUBASSY\_STEEL

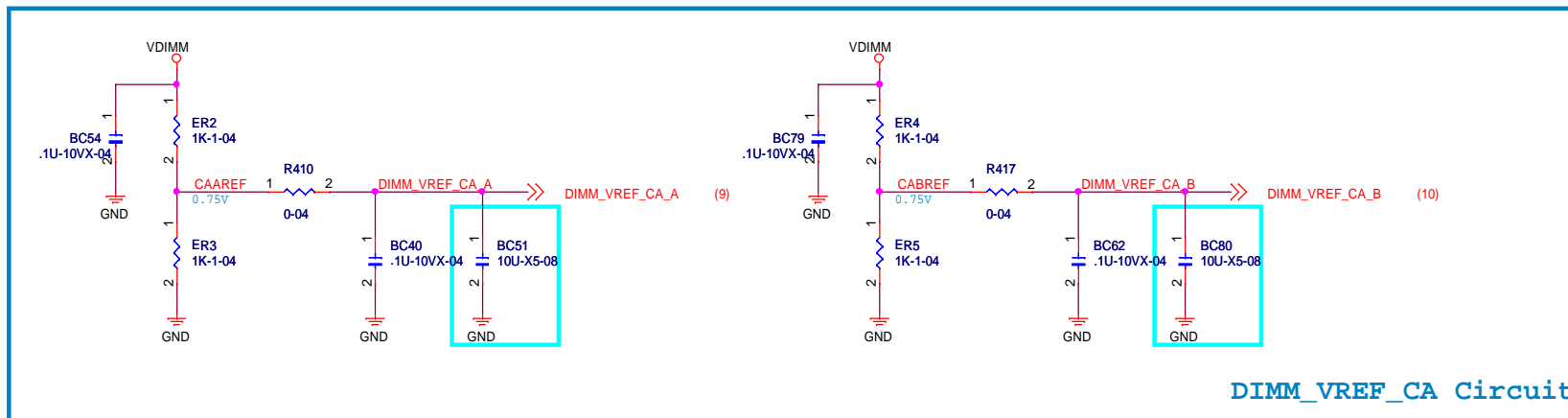
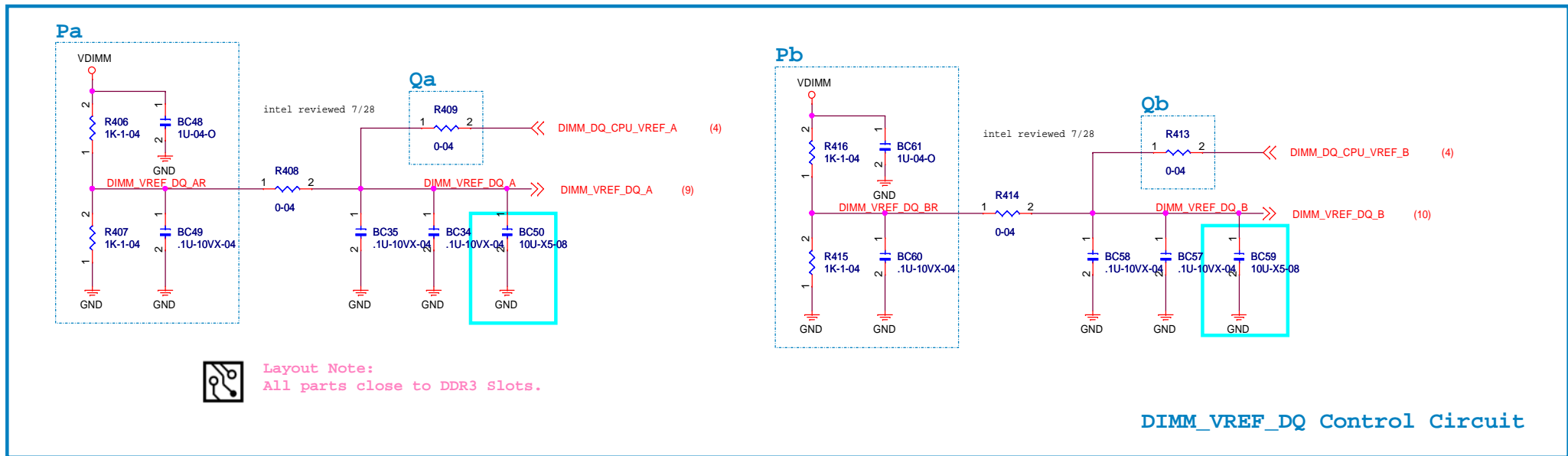


<b>CPU - GND, CPU_RST_L</b>	
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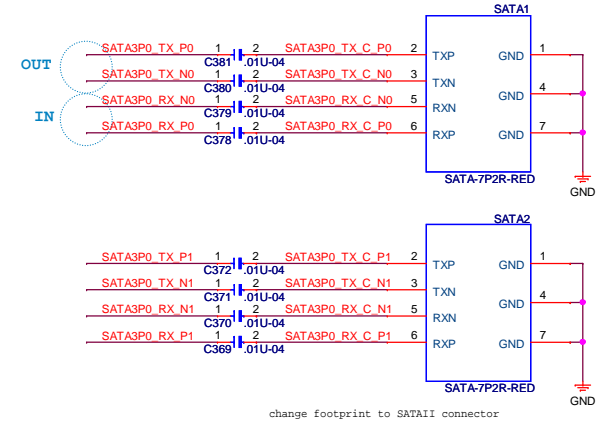
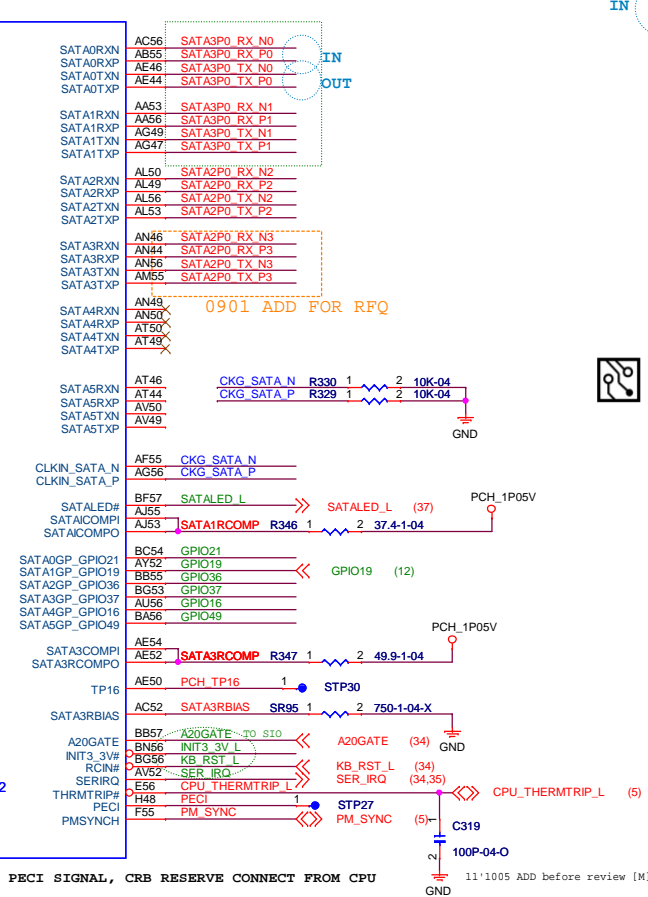
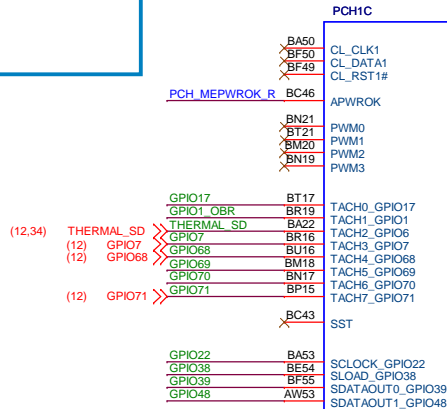
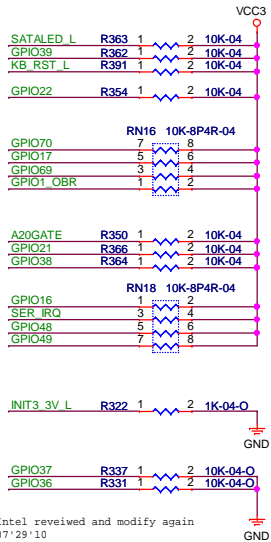
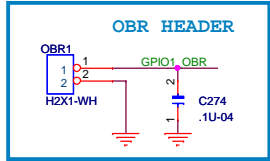
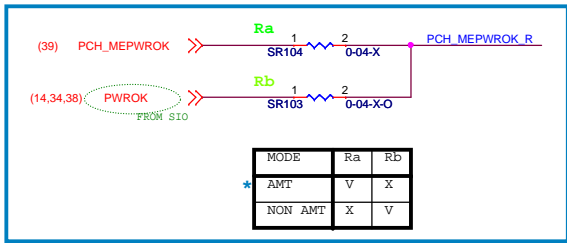








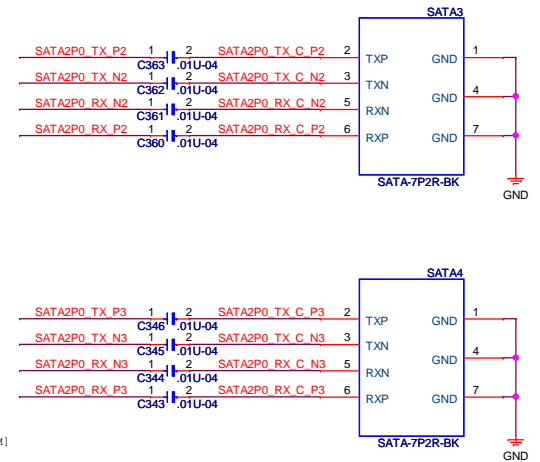




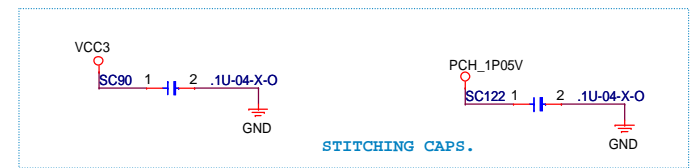
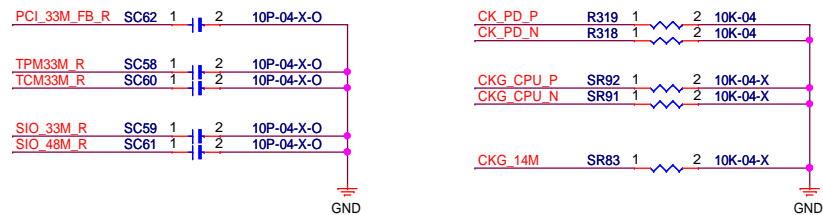
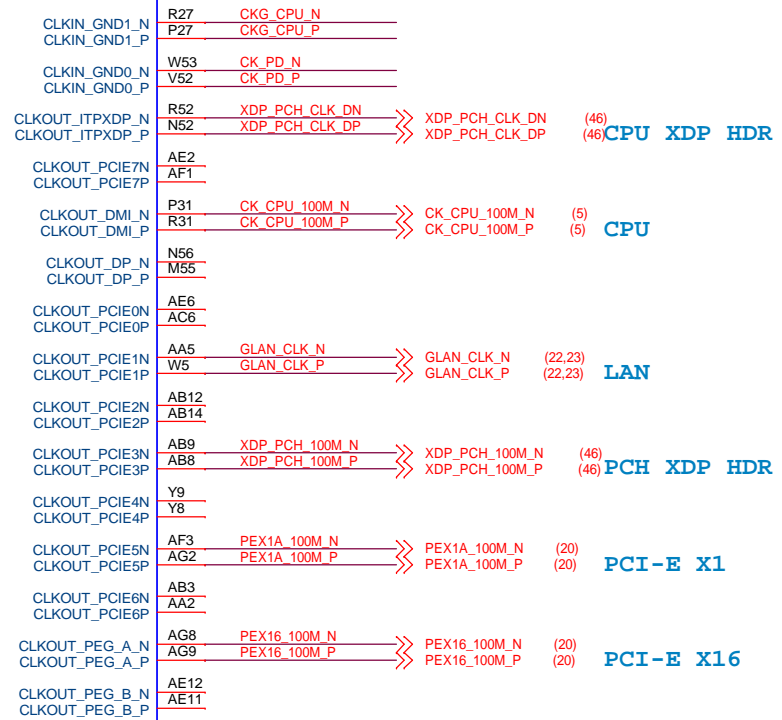
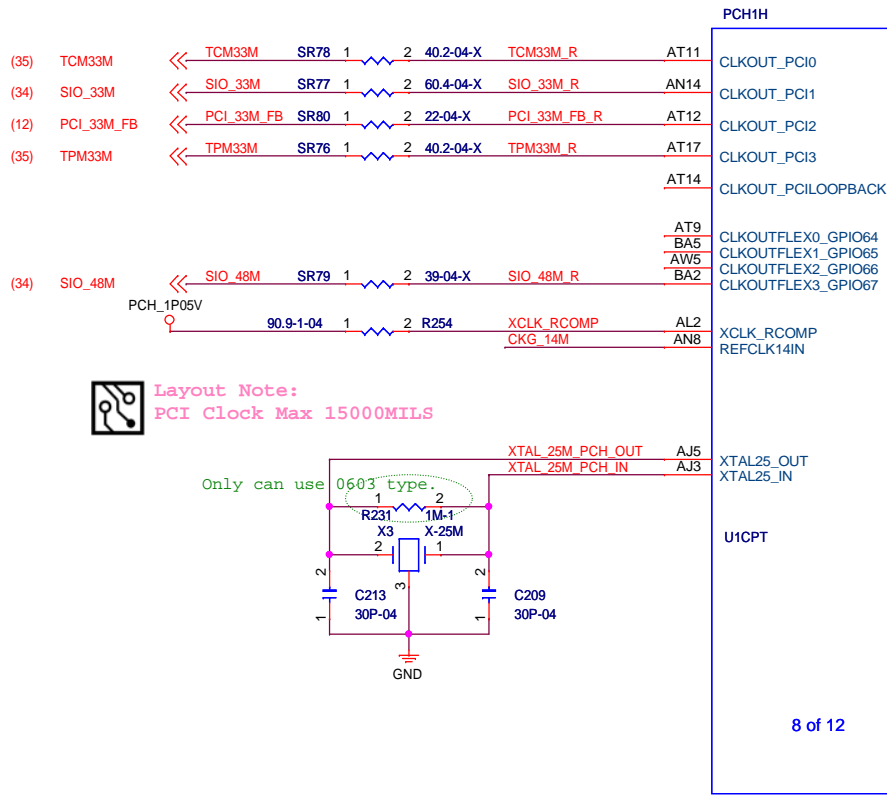
Layout Note:

SATA3.0 4.5/7.5/20 in 90 Ω ±17.5%

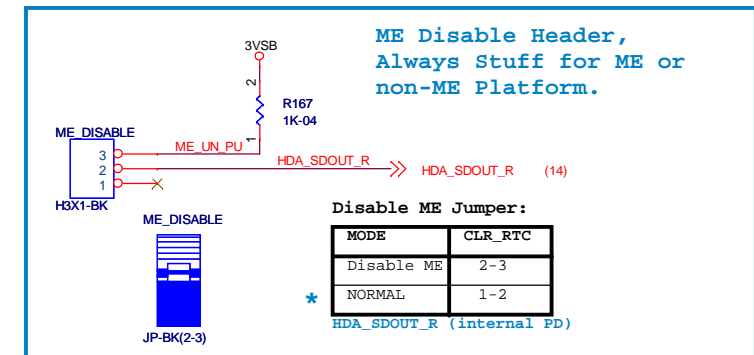
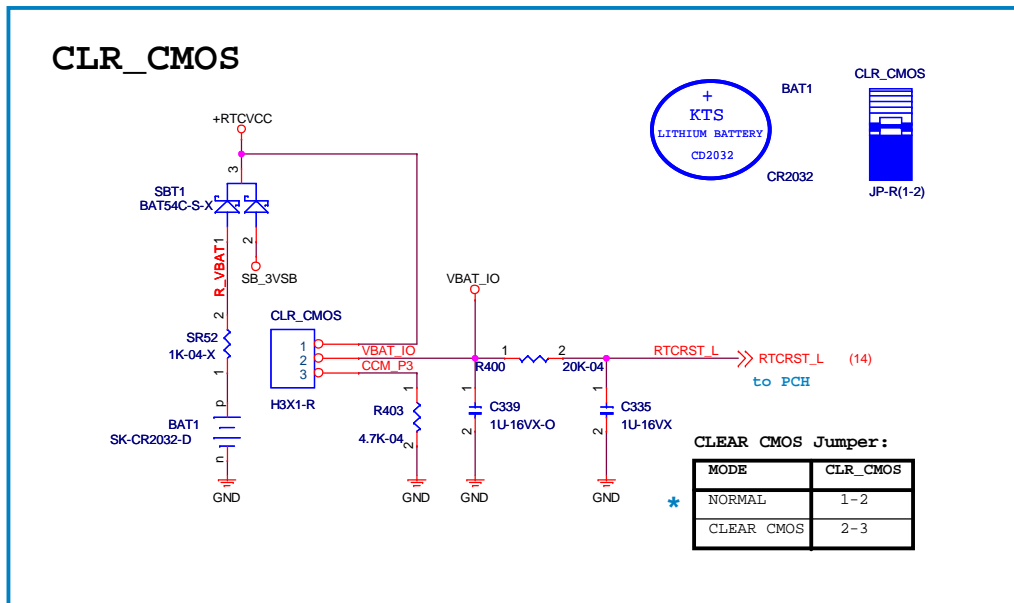
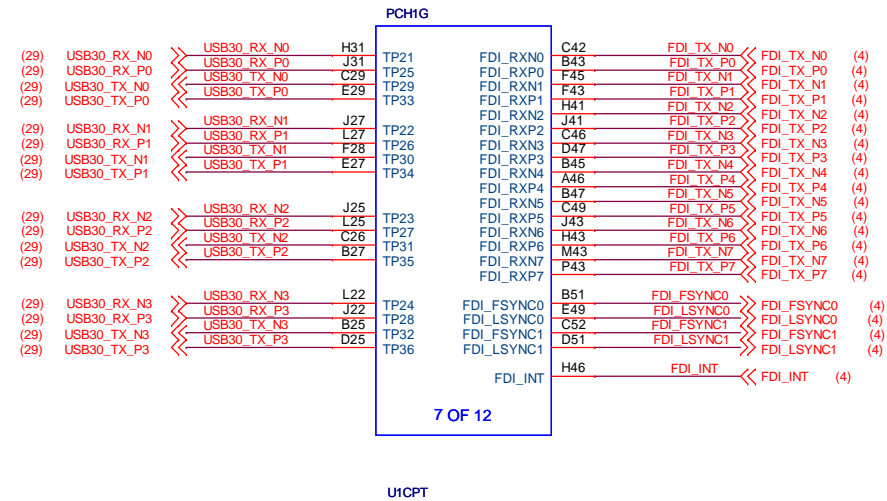
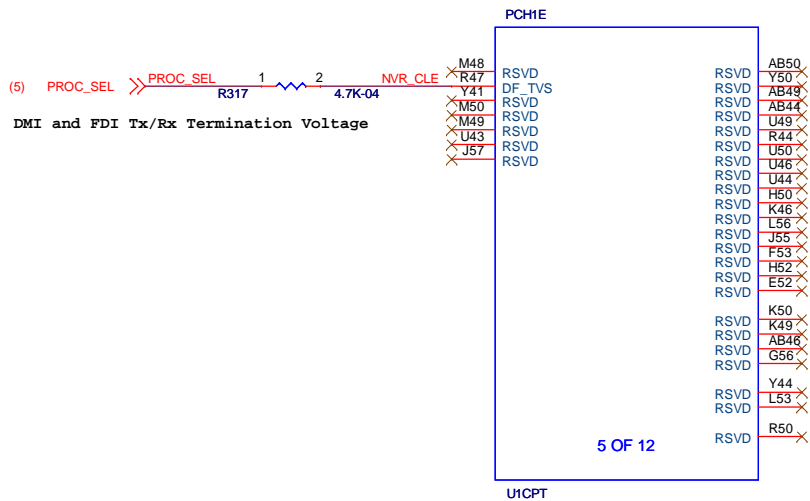
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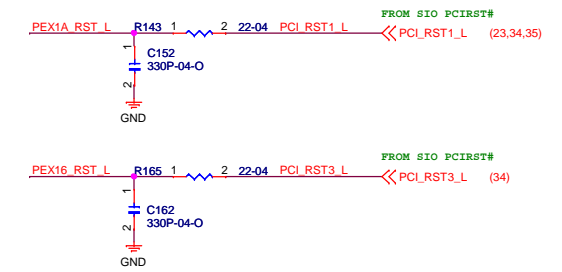
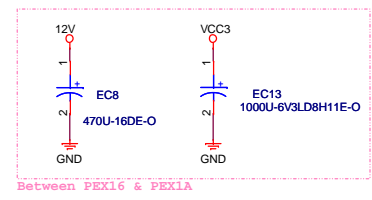
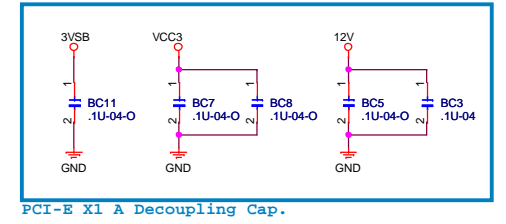
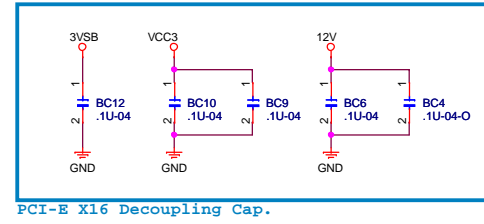
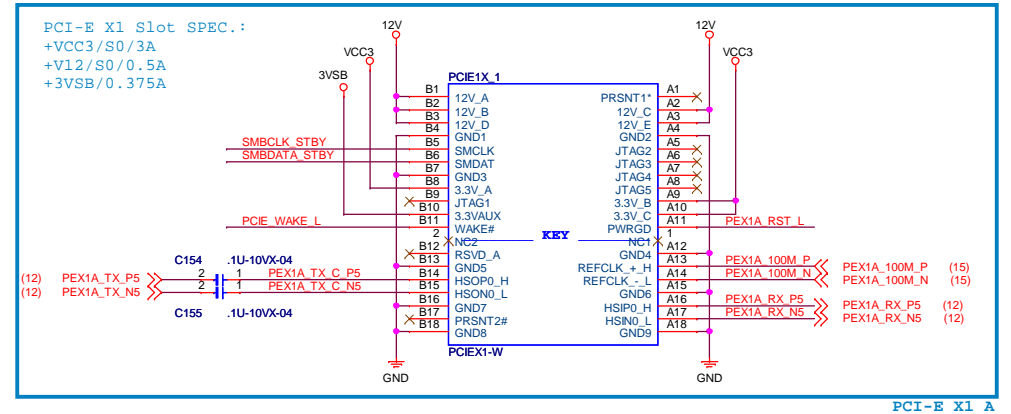




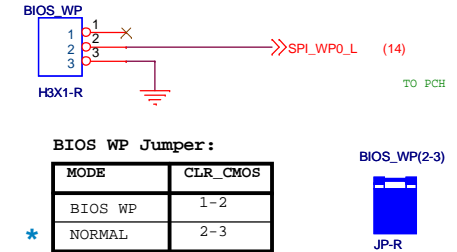
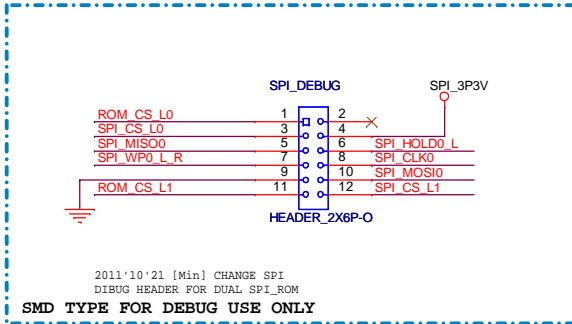
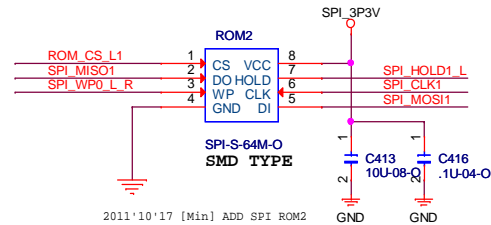
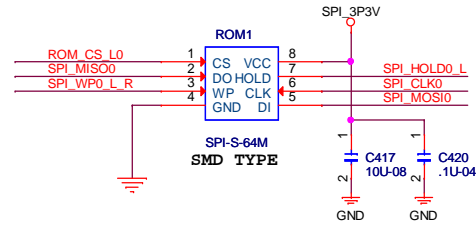
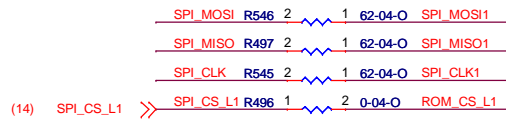
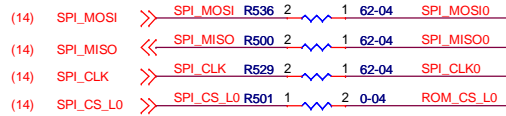
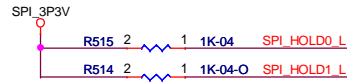
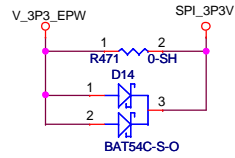




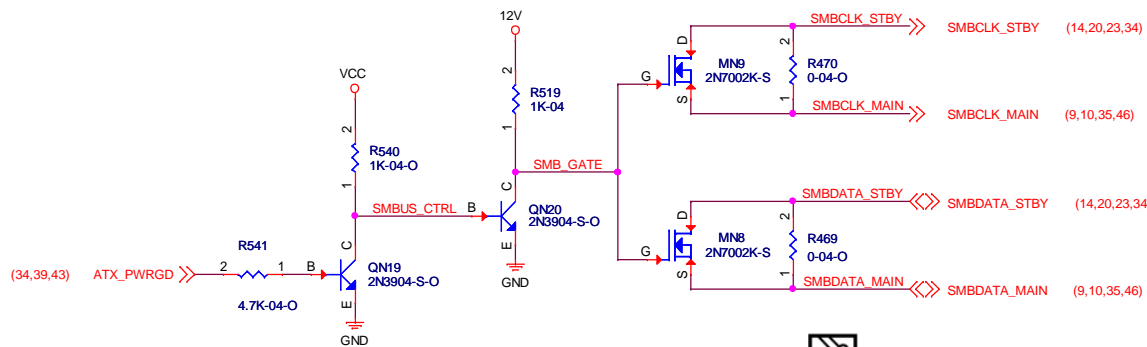
PCI-E X16 Slot SPEC.:  
+VCC3/S0/3A  
+V12/S0/5.5A  
+3VSB/0.375A



## SPI ROM Circuit



## SMBUS Logic Circuit



Layout Note:  
SMBUS Trace Max 21500MILS



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Title  
SBI ROM, SMBUS

Size  
Custom

Document Number  
Q77H2-AD

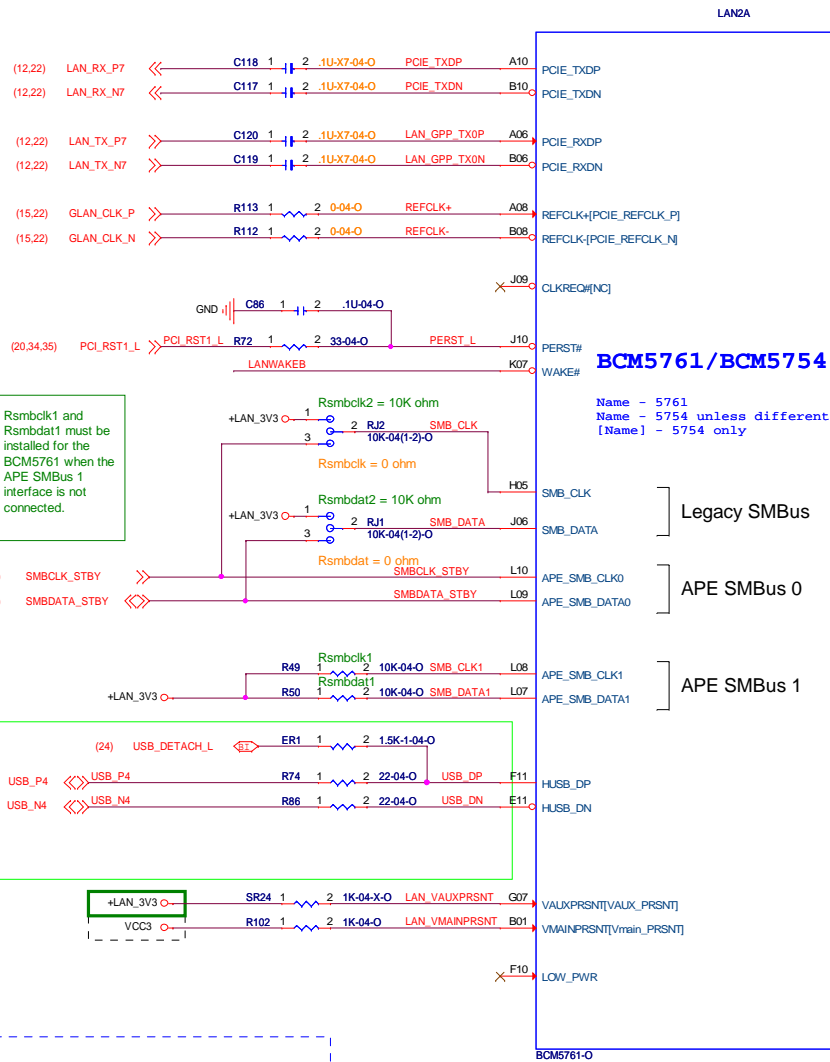
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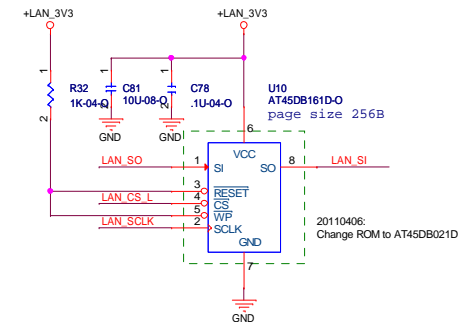
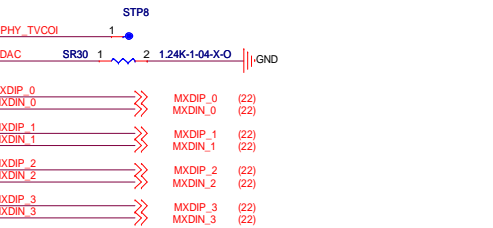




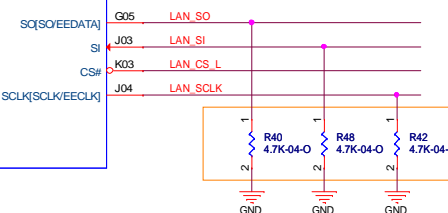
Rsmblck and Rsmmdat must be installed for the BCM5754 only.

Rsmblck2 and Rsmmdat2 must be installed for the BCM5761 only.

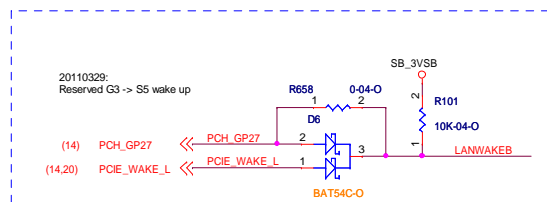
Rsmblck1 and Rsmmdat1 must be installed for the BCM5761 when the APE SMBus 1 interface is not connected.

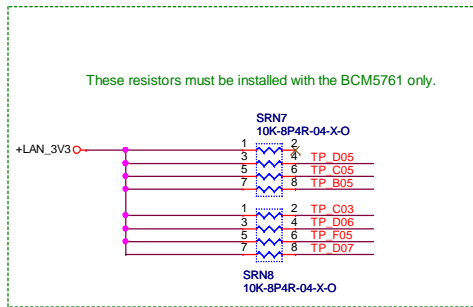


Flash device shown is for the BCM5761 only. Refer to the BCM5754 data sheet for supported flash devices.



These resistors must be installed with the BCM5754 to configure flash auto-sense.





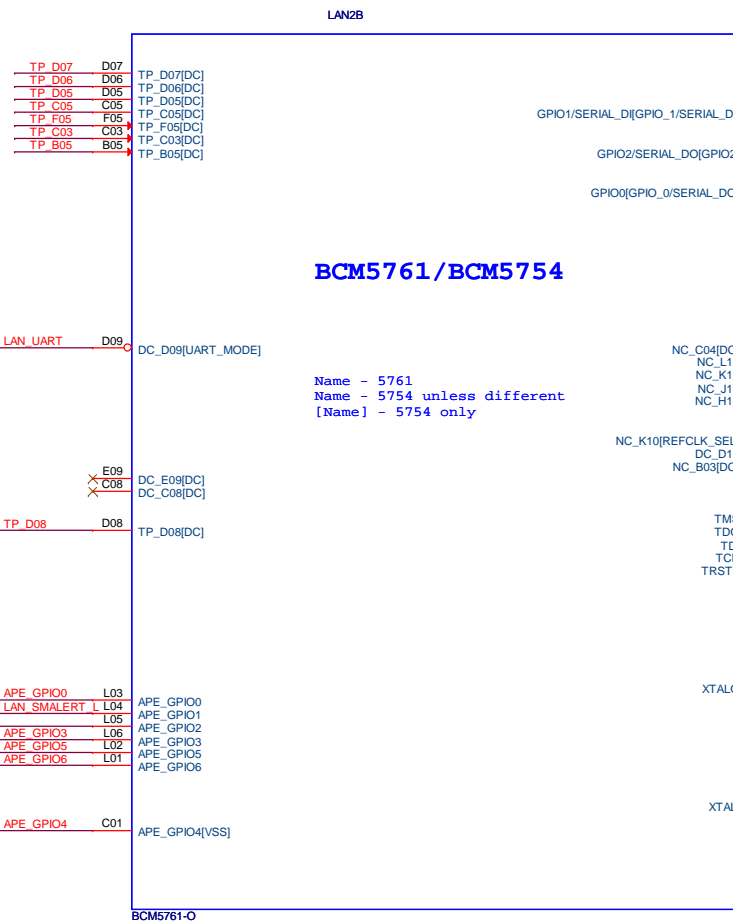
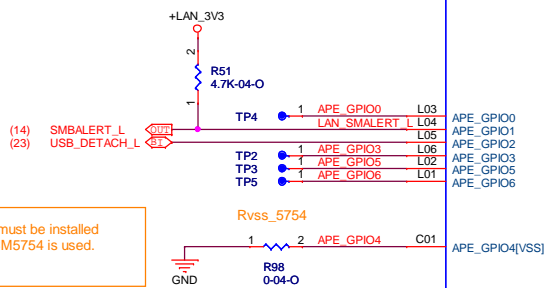
Ruart\_mode should be installed to enable the debug UART function when the BCM5754 is used.



Rd8\_pd must be installed with the BCM5761 only.



Rvss\_5754 must be installed when the BCM5754 is used.



## BCM5761/BCM5754

Name - 5761  
Name - 5754 unless different  
[Name] - 5754 only

Rsmalert# should be installed when the BCM5754 ASF doorbell function is used.

For Energy Detection function use only for 5761E use

Rrefcksel must not be installed with the BCM5761, but may be installed with the BCM5754

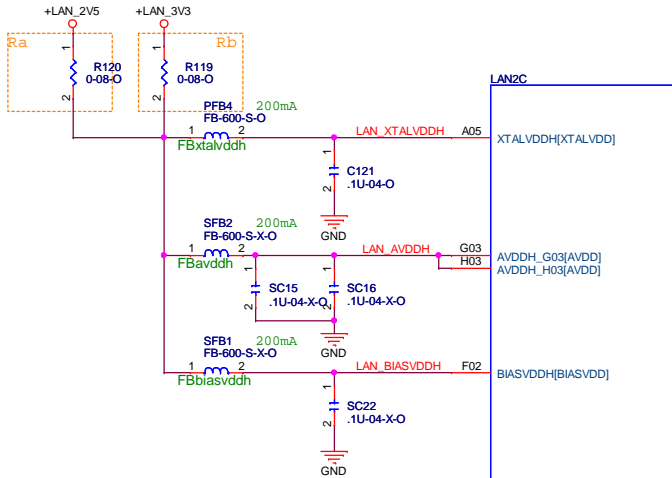
**Elitegroup Computer Systems**

Title: **LAN (BCM5761) XTAL,GPIO**

Size: Custom Document Number: **Q77H2-AD** Rev: 1.0

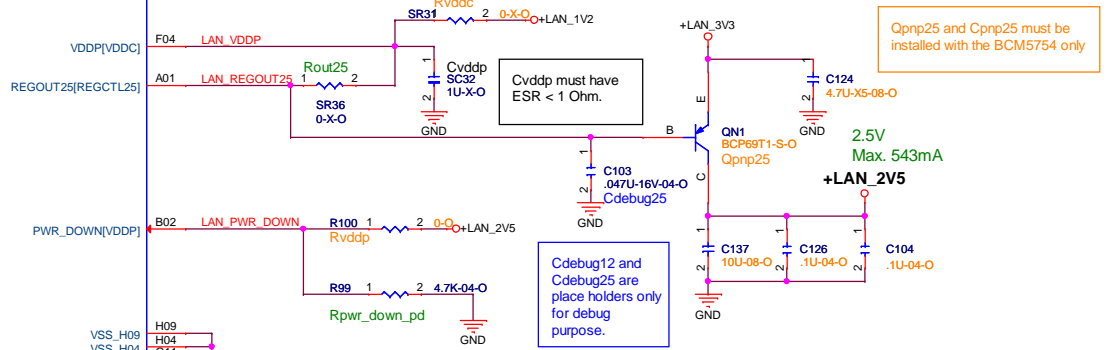
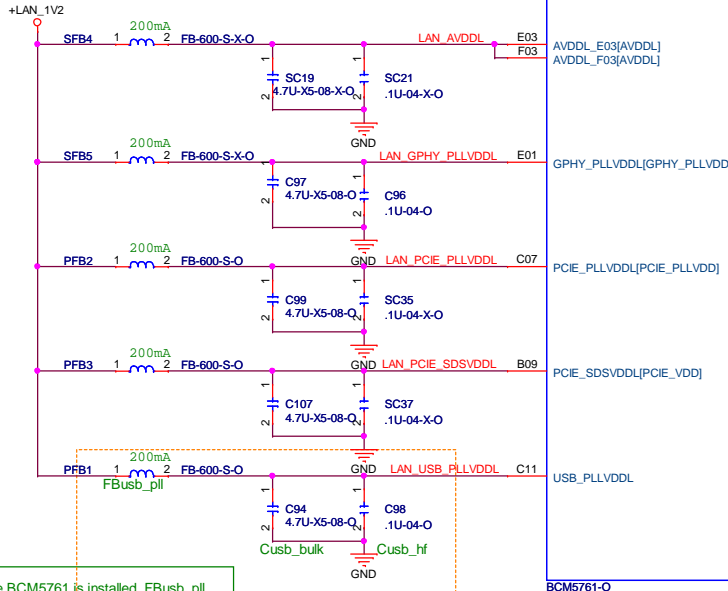
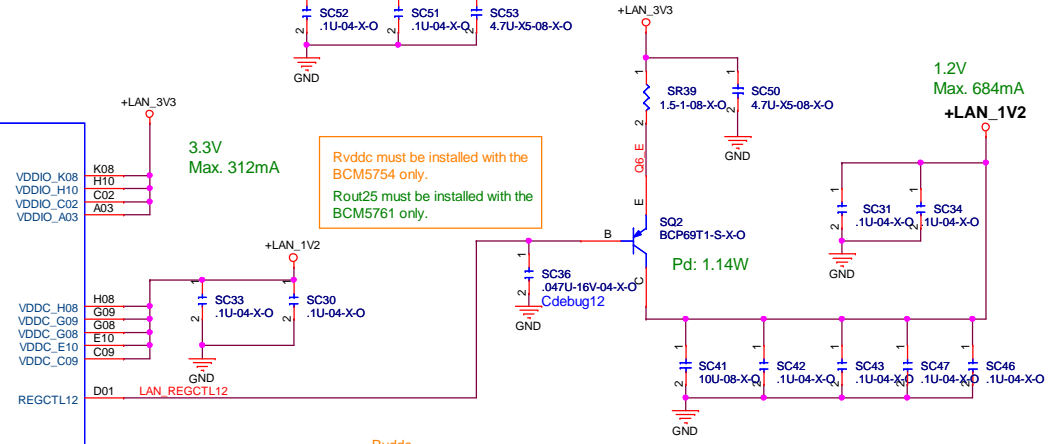
Date: Tuesday, April 10, 2012 Sheet: 24 of 49

	5754	5761
Ra	V	X
Rb	X	V



## BCM5761/BCM5754

Name - 5761  
Name - 5754 unless different  
[Name] - 5754 only



If the BCM5761 is installed, FBusb\_pll, Cusb\_bulk, and Cusb\_hf must be laid out even if the USB interface is not used since the USB PLL may provide an alternate clock source internal to the BCM5761.

If the BCM5754 is installed, FBusb\_pll, Cusb\_bulk, and Cusb\_hf may be uninstalled.

Rvddc must be installed with the BCM5754 only.

Rpwr\_down\_pd must be installed with the BCM5761 only.

The PWR\_DWN[VDDP] ball must not be driven to 3.3V. Refer to the BCM5761 data sheet for logic thresholds and maximum ratings.

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Title

**LAN (BCM5761) PWR & GND**

Size Custom

Document Number

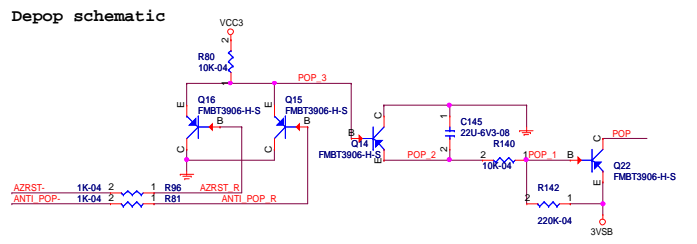
**Q77H2-AD**

Date: Tuesday, April 10, 2012

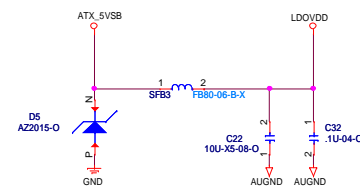
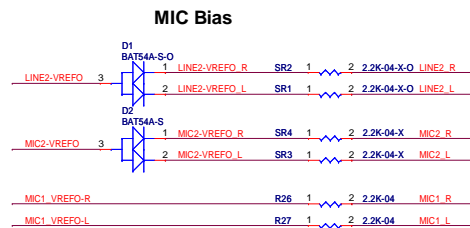
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Rev 1.0

Depop schematic

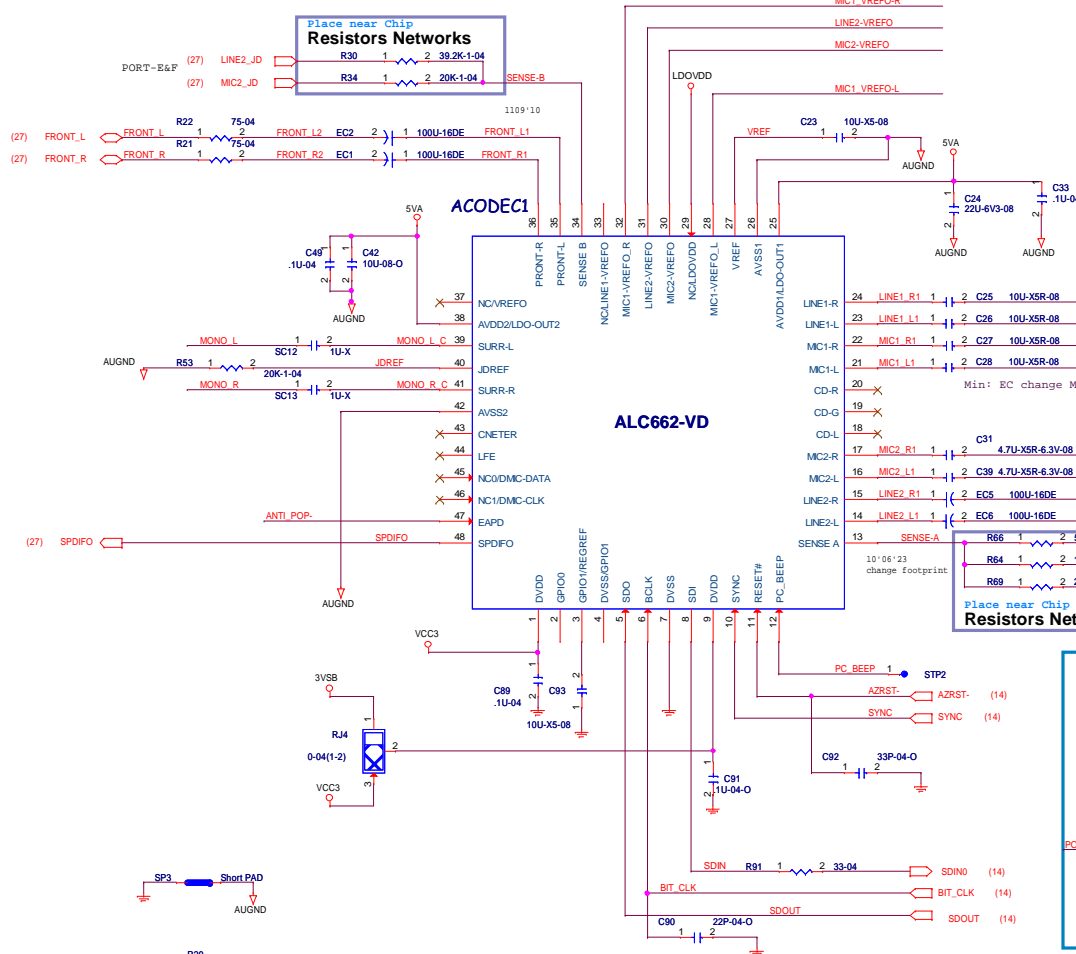


## MIC Bias

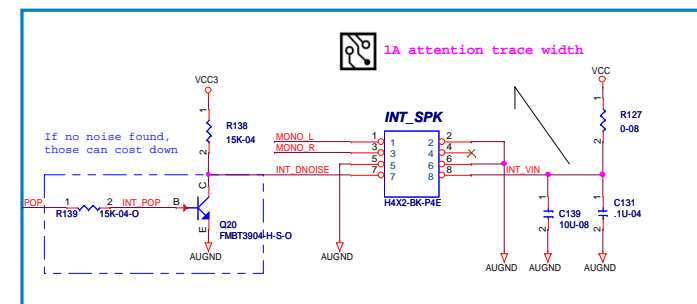
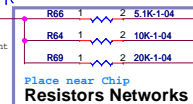


## Place near Chip

# Resistors Networks

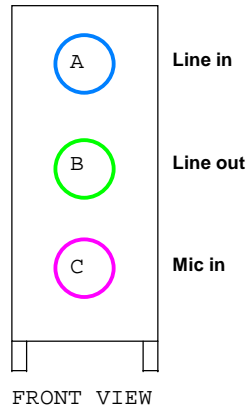
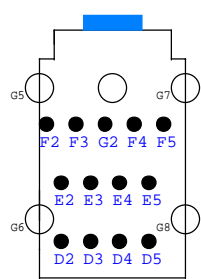
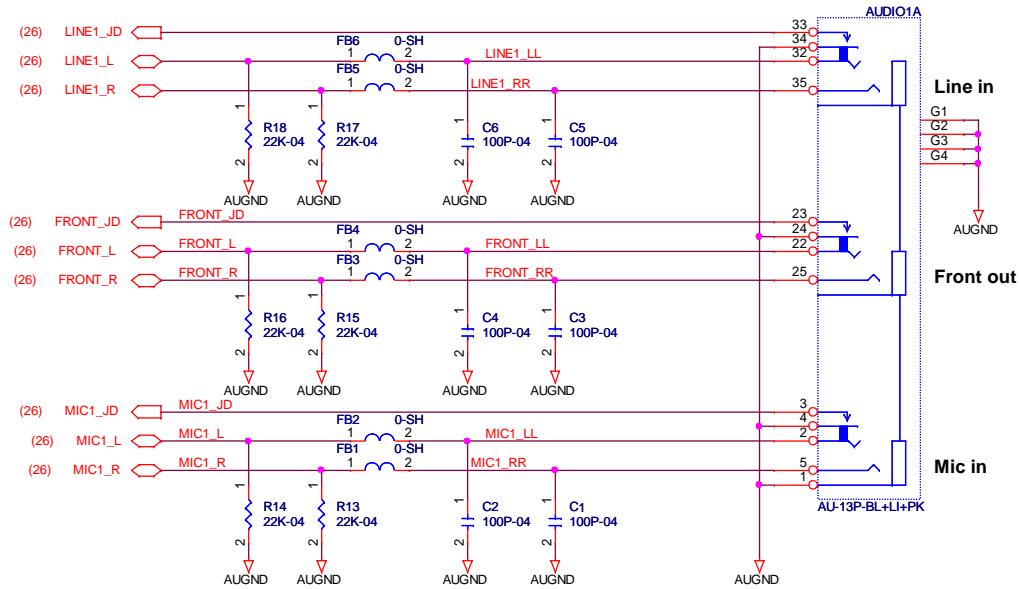


**ALC662-VD**

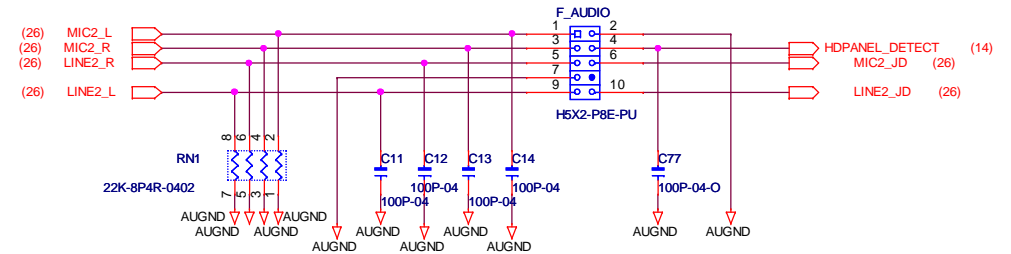


"INTERNAL SPEAKER"  
FOR COMMERCIAL AND AIO SERIES USE

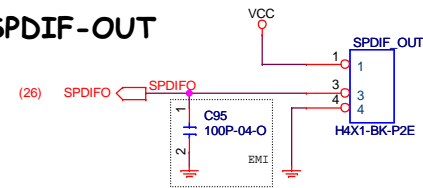
## REAR-AUDIO



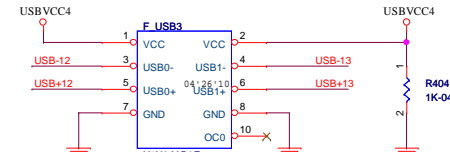
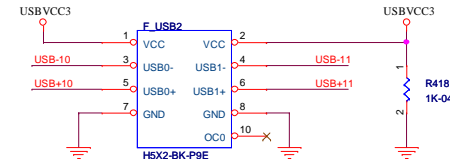
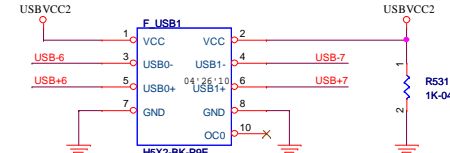
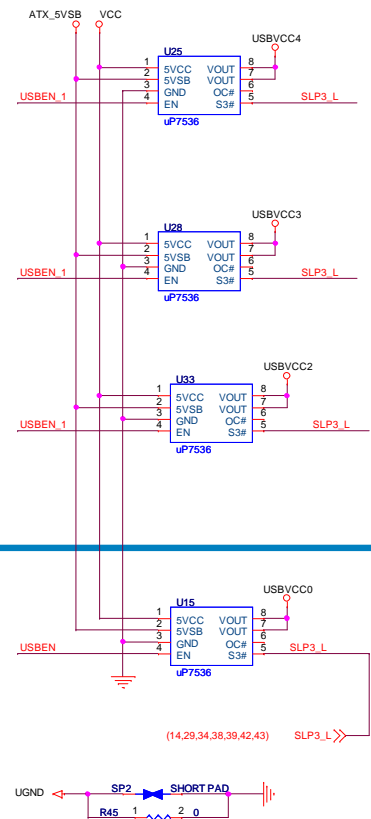
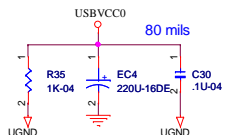
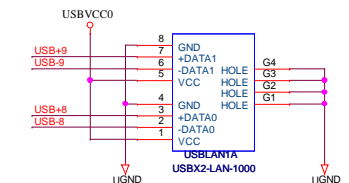
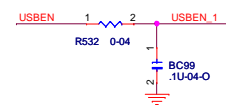
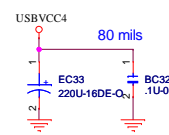
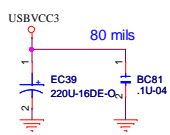
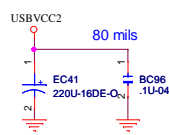
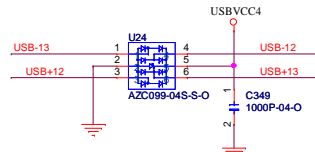
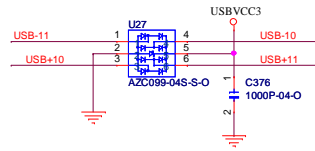
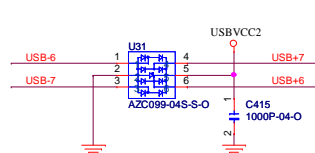
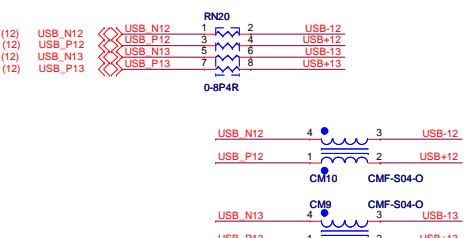
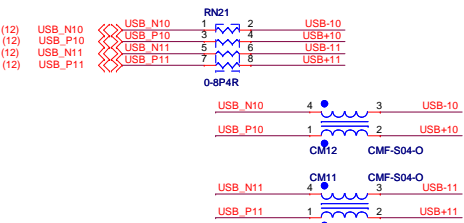
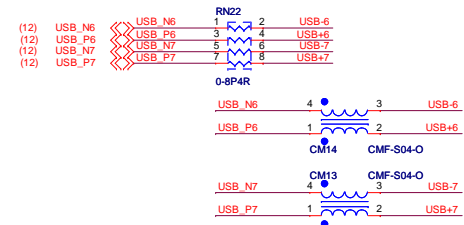
## FRONT-AUDIO



## SPDIF-OUT



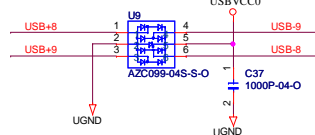
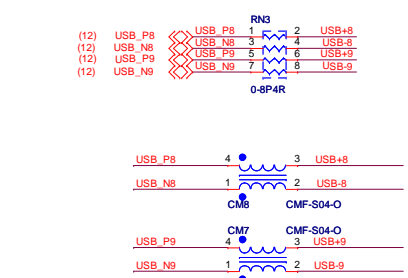
<b>AUDIO ALC662 Connector (PANEL)</b>	
<b>Size B</b>	<b>Document Number</b> <b>Q77H2-AD</b>
<b>Date:</b> Tuesday, April 10, 2012	<b>Rev</b> 1.0
<b>Sheet</b> 27	<b>of</b> 49

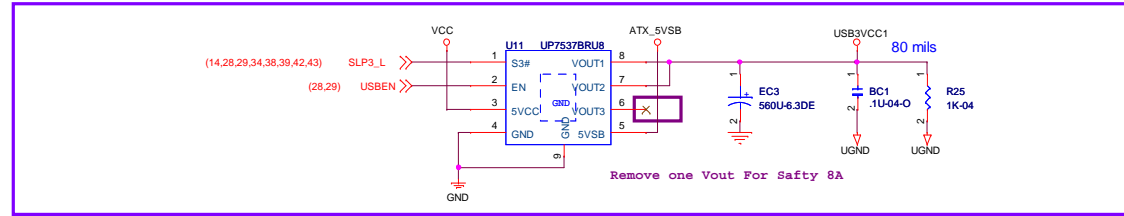
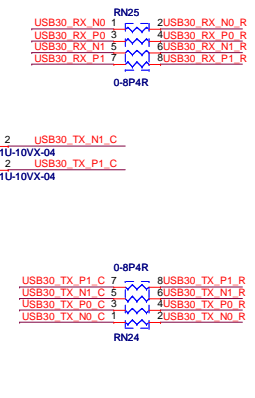
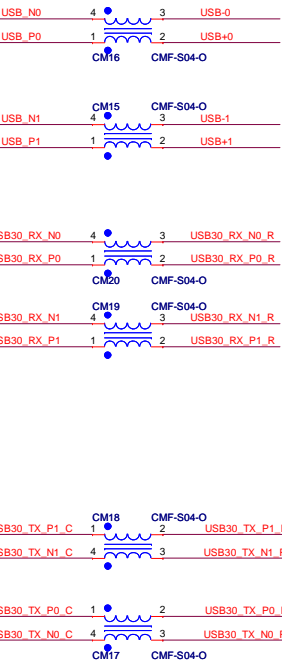
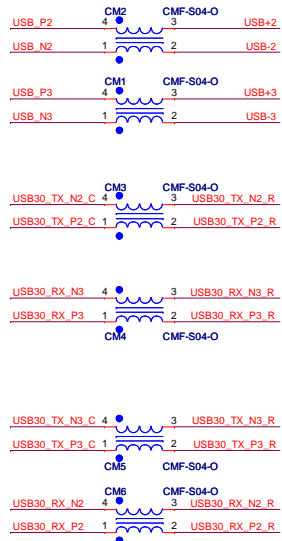
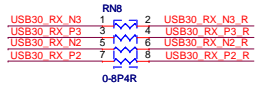
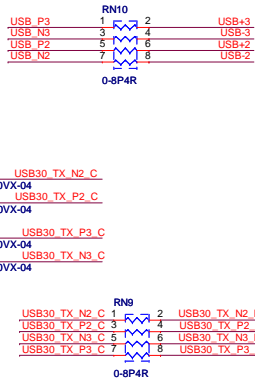
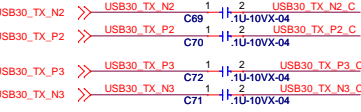
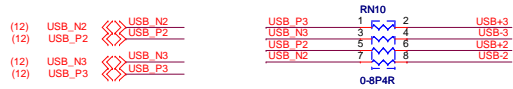


	uP7536 Enable use	Ra	Rb	Rb	S4/S5 USB_5V_DUAL	Customer
	VDIMM	0ohm	N A	N A	0 Volt	Acer CONSUMER
*	PCH GPIO72 default High	N A	100ohm	N A	BIOS CONTROL	Acer COMMERCIAL
	PCH GPIO24 default Low	N A	N A	100ohm	BIOS CONTROL	Acer COMMERCIAL

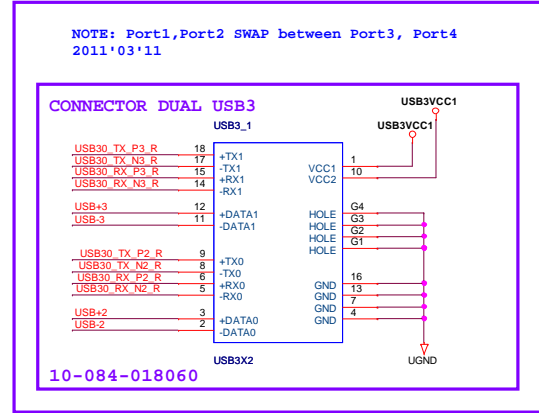
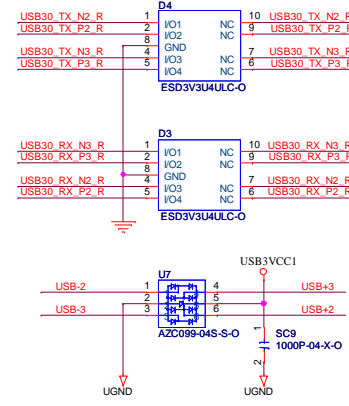
**FRONT PANEL USB2.0 HEADER**

**REAR PANEL USB2.0 CONNECTOR**



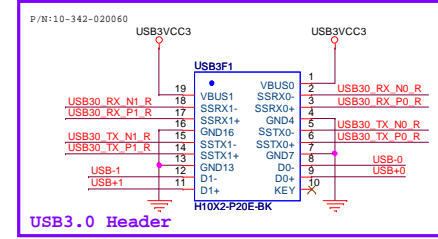
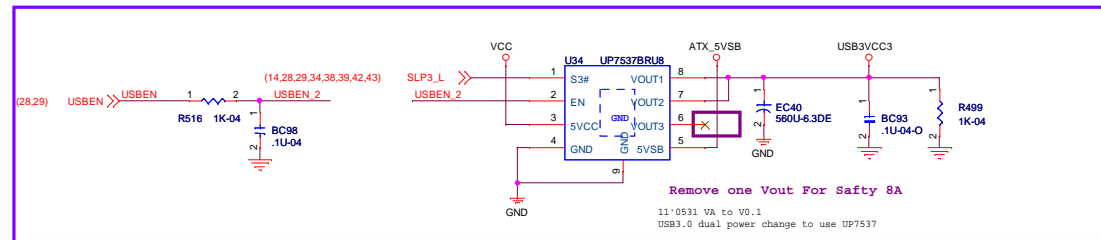


# USB3 ESD COMPONENTS



## REAR PANEL USB3.0 CONNECTOR

## FRONT PANEL USB3.0 HEADER



## USB3 ESD COMPONENTS

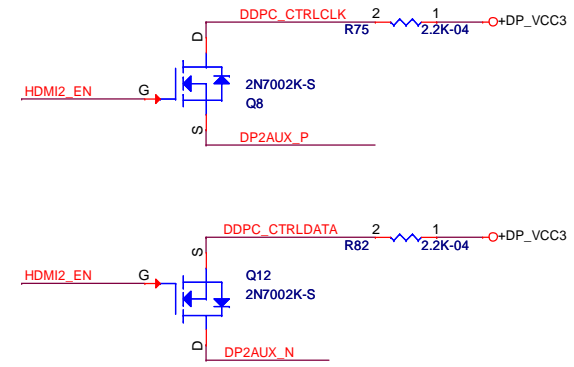
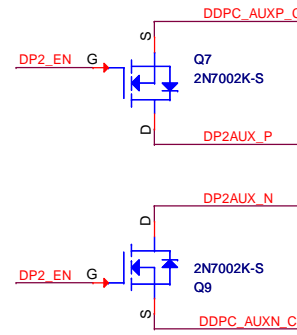
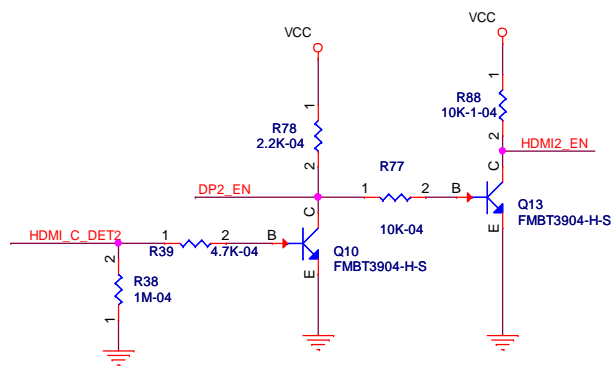
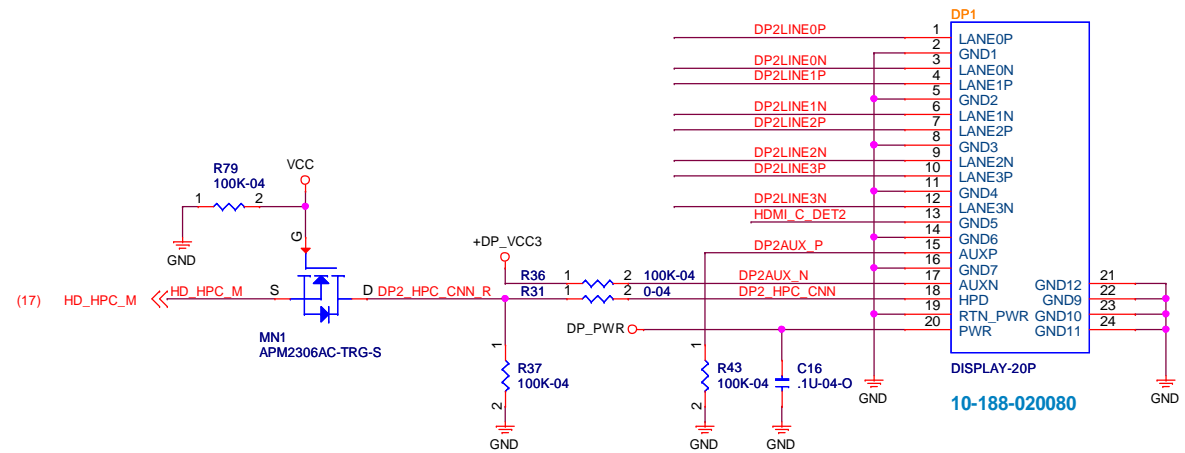
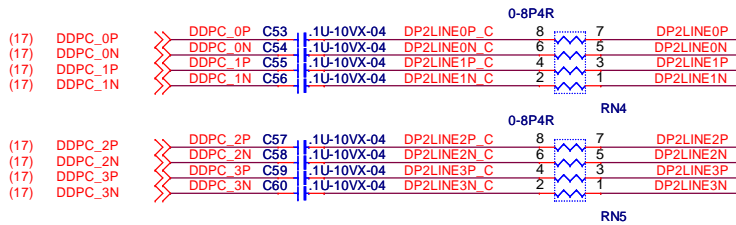
Elitegroup Computer Systems

Title			USB3.0 Connector
Size	Document Number	Q77H2-AD	
Custom			
Date:	Tuesday, April 10, 2012	Sheet	29 of 49
		Rev	1.0



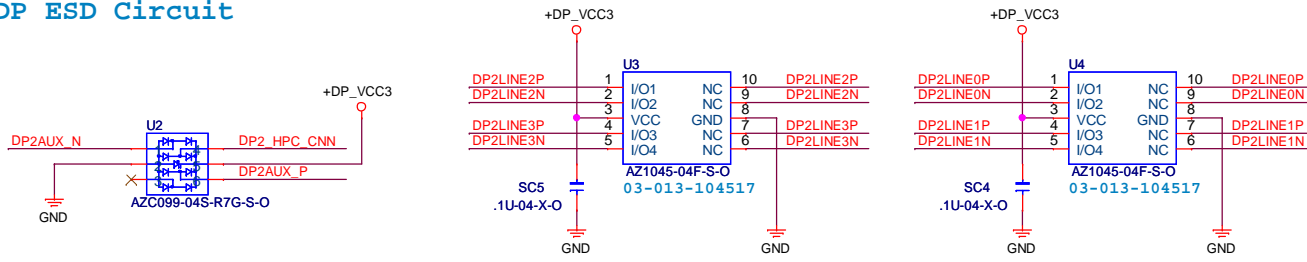
(17) DDPC\_CTRLDATA >> DDPC\_CTRLDATA  
(17) DDPC\_CTRLCLK >> DDPC\_CTRLCLK

(17) DDPC\_AUXP >> DDPC\_AUXP C44 :1U-10VX-04 DDPC\_AUXP\_C  
(17) DDPC\_AUXN >> DDPC\_AUXN C41 :1U-10VX-04 DDPC\_AUXN\_C



SUPPORT DP TO HDMI/DVI DONGLE

## DP ESD Circuit



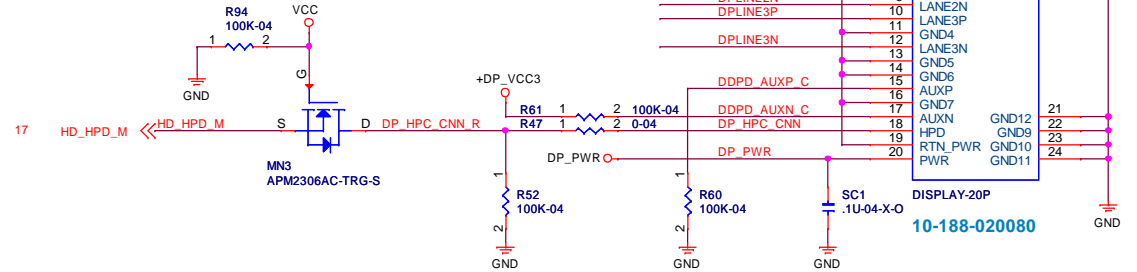
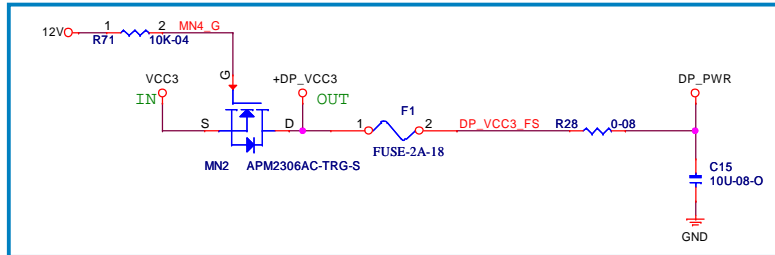
**ECS** Elitegroup Computer Systems

Title			DISPLAY PORT1
Size	Document Number	Rev	
Custom	Q77H2-AD	1.0	
Date:	Tuesday, April 10, 2012	Sheet	30 of 49

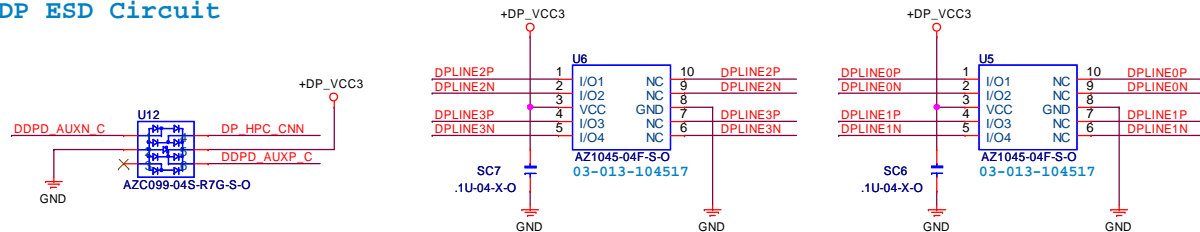
DDPD\_AUXP >> DDPD\_AUXP C80 >> 1U-10VX-04 DDPD\_AUXP\_C  
DDPD\_AUXN >> DDPD\_AUXN C79 >> 1U-10VX-04 DDPD\_AUXN\_C

DDPD\_0P >> DDPD\_0P C61 >> 1U-10VX-04 DPLINE0P\_C 8 7 DPLINE0P  
DDPD\_0N >> DDPD\_0N C62 >> 1U-10VX-04 DPLINE0N\_C 6 5 DPLINE0N  
DDPD\_1P >> DDPD\_1P C63 >> 1U-10VX-04 DPLINE1P\_C 4 3 DPLINE1P  
DDPD\_1N >> DDPD\_1N C64 >> 1U-10VX-04 DPLINE1N\_C 2 1 DPLINE1N

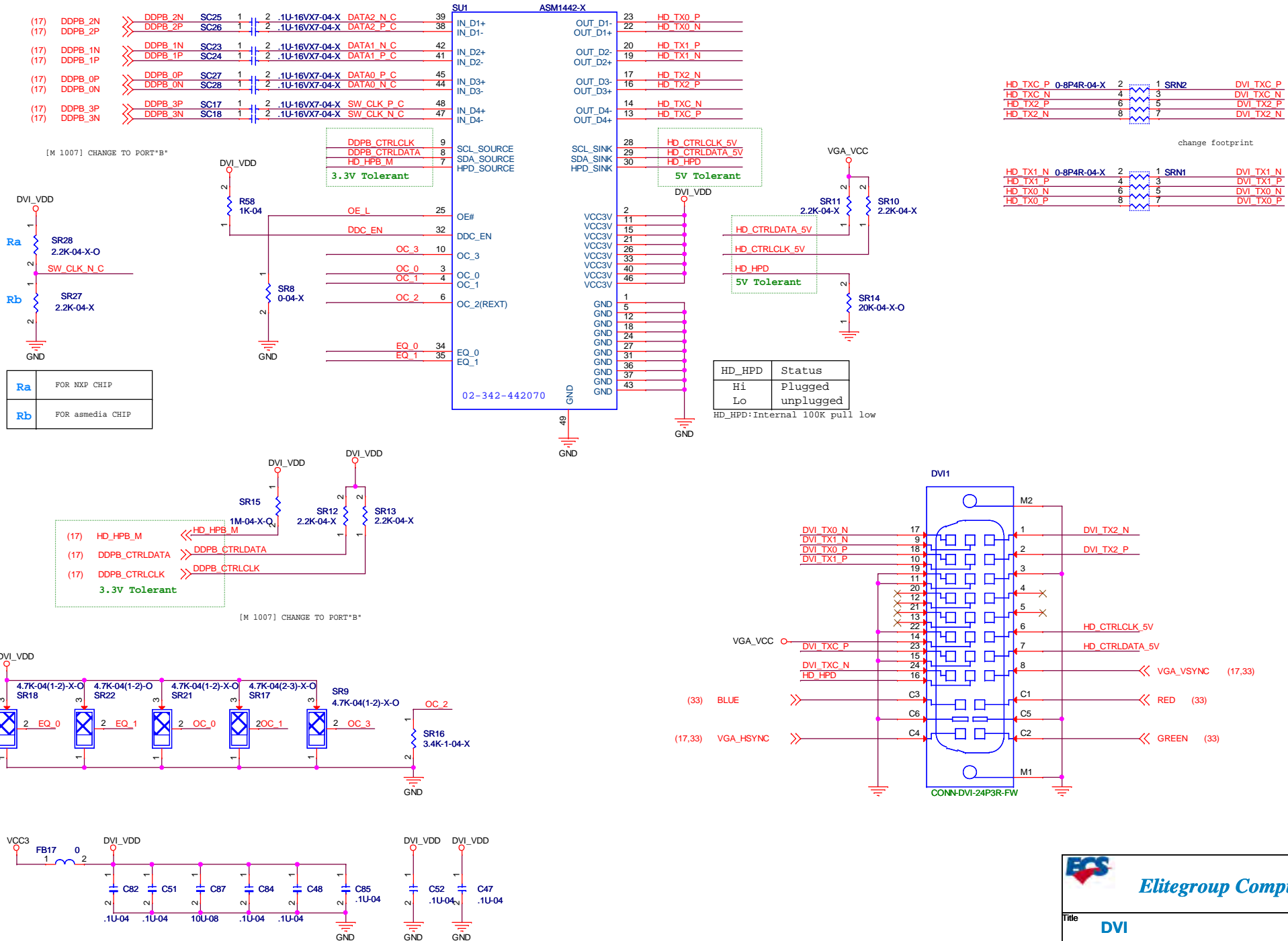
DDPD\_2P >> DDPD\_2P C65 >> 1U-10VX-04 DPLINE2P\_C 8 7 DPLINE2P  
DDPD\_2N >> DDPD\_2N C66 >> 1U-10VX-04 DPLINE2N\_C 6 5 DPLINE2N  
DDPD\_3P >> DDPD\_3P C67 >> 1U-10VX-04 DPLINE3P\_C 4 3 DPLINE3P  
DDPD\_3N >> DDPD\_3N C68 >> 1U-10VX-04 DPLINE3N\_C 2 1 DPLINE3N

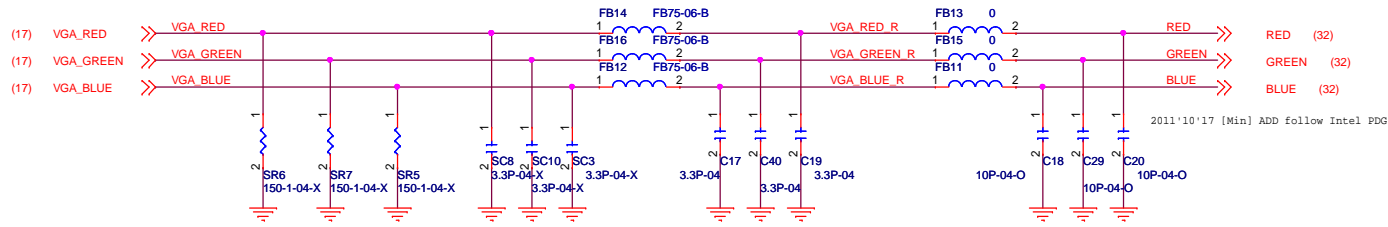


## DP ESD Circuit

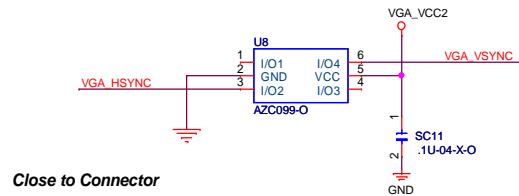
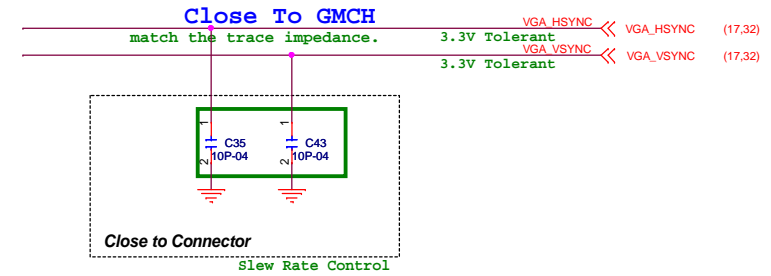


# Level Shifter

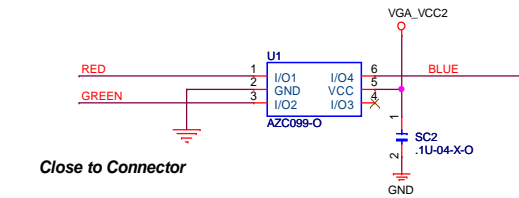




**Close to Connector**

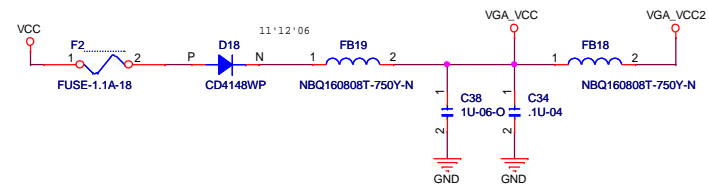


**Close to Connector**

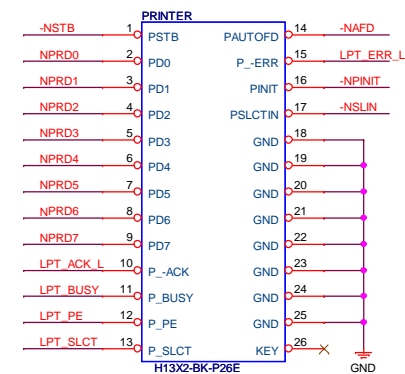


**Close to Connector**

If build in Internal DVI Con,  
that can use the circuit to protect reverse voltage together.

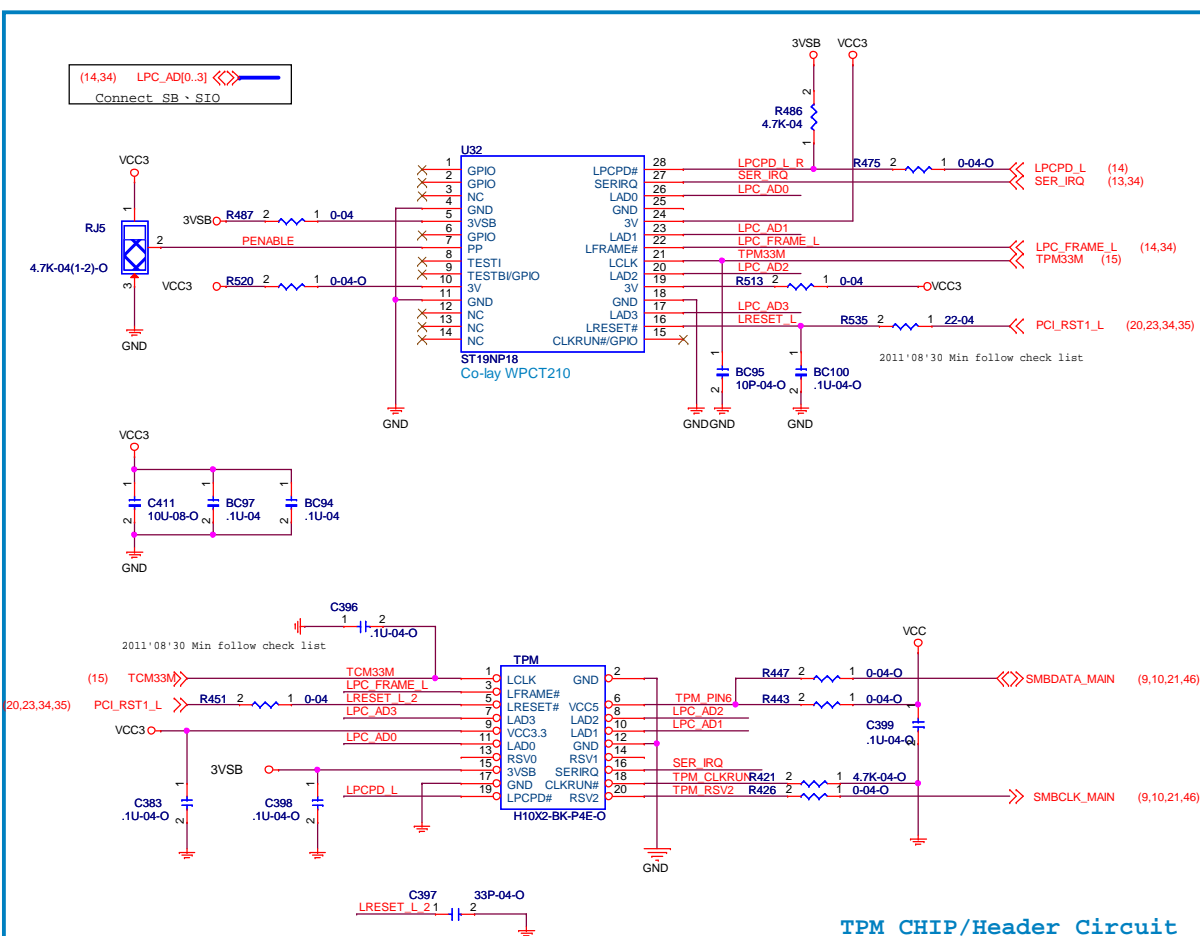




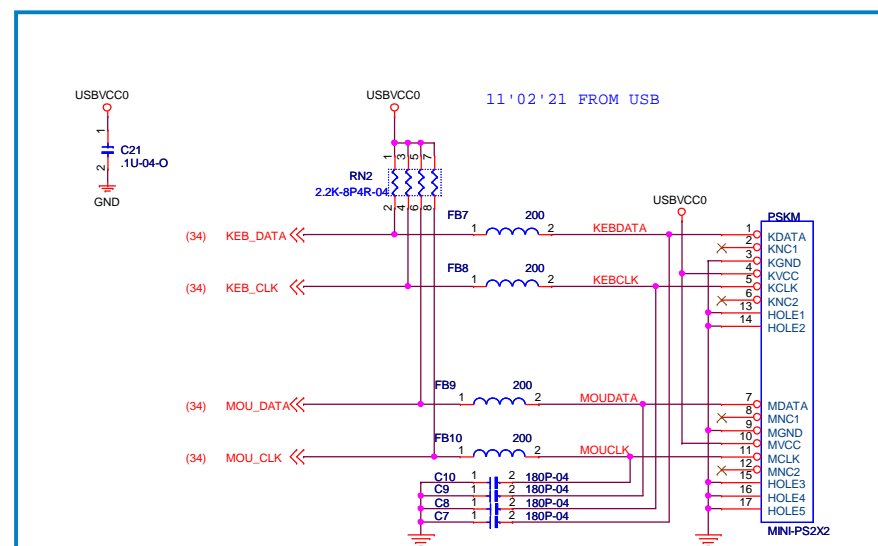


0901 CHANGE FOR RFQ

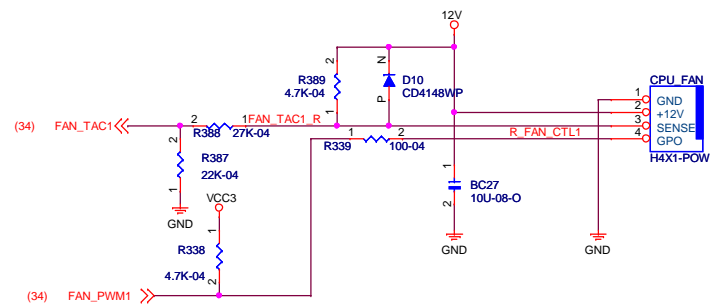
## LPT Header Circuit



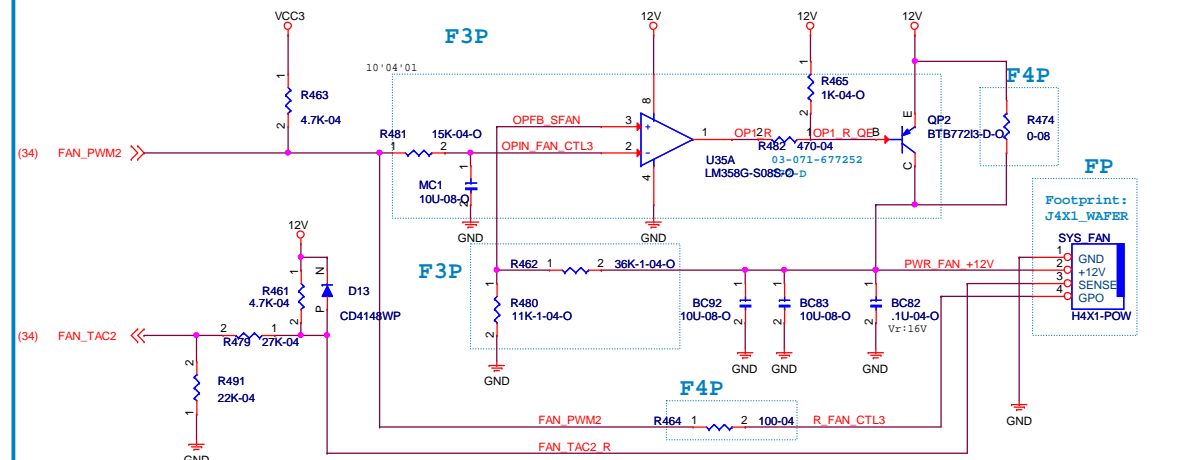
## TPM CHIP/Header Circuit



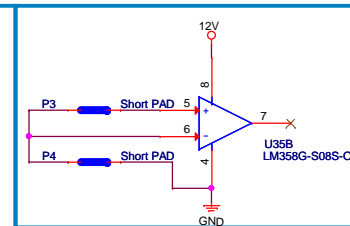
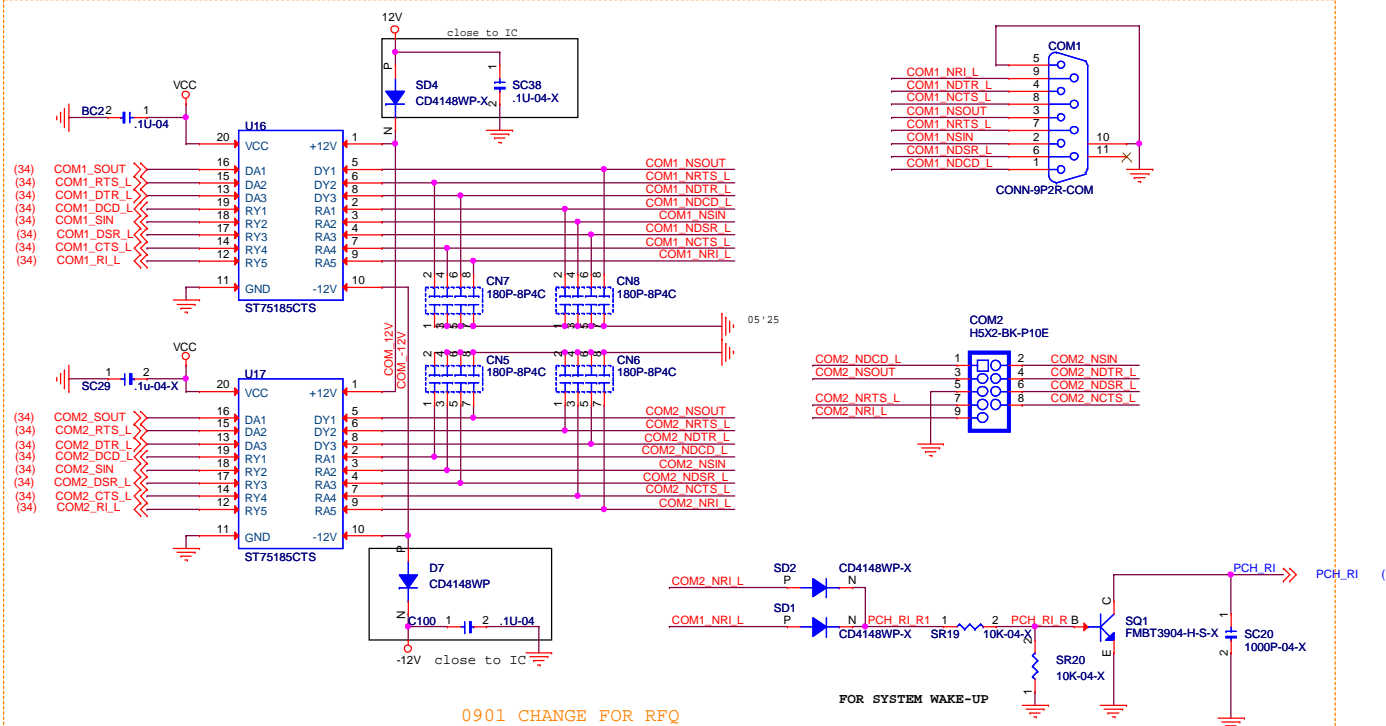
## PS2-KB Circuit



## CPU FAN 4-PIN Circuit



### SYS FAN 3-PIN(Co-Lay 4PIN) Circuit



MODE	F3P	F4P	FP Value
3PIN	V	X	H3X1-P-W
4PIN	X	V	H4X1-P-W

0901 CHANGE FOR RFQ

+ - terminal add short pad to ground for nonuse OP , 20110406



### Front Panel Circuit

2011'08'24 require 10K pull up

(13) SATALED\_L  
(5,14,46) SYS\_RST\_L

(22) LAN\_LED0\_ACTIVE

(34,46) SIO\_PWRBTN\_L

(34) SIO\_LED0

(14,34,40) SLP4\_L

LED CT

GLEDO0, GLED1 Current = 13mA < 20mA(If)  
R443, R444 Power = 56mW < 62.5mW(R0402)

# Buzzer Circuit

The diagram illustrates a Buzzer Circuit. It features two input signals: (34) SIO\_BEEP and (14) PCH\_SPKR. SIO\_BEEP is connected to a network of a 1K-04 resistor (R574) and a .1U-04 capacitor (C433) to VCC. PCH\_SPKR is connected to a 1K-04 resistor (R568) and a BZQ\_B node. BZQ\_B is connected to the base of a BJT transistor (Q32, FMBT3904-H-S) and the emitter of a diode (D15, CD4148WP). The diode's anode is connected to VCC. The collector of the transistor is connected to a BZQ\_C node, which is also connected to a 120-08 resistor (R556) and the anode of a buzzer (BZ1, BUZZER-D). The buzzer's cathode is connected to ground through a .1U-04 capacitor (C432).

MODIFY Ra/Rb VALUE FOR FOLLOWING RULES  
1)AC ON: 3VSB vs RSMRST(t204: min 10ms)  
2)AC OFF: 3VSB>2.9V when RSMRST<0.8V



05'09'10

2

ER7

110K-1-04-O

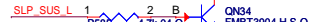
0.82 V

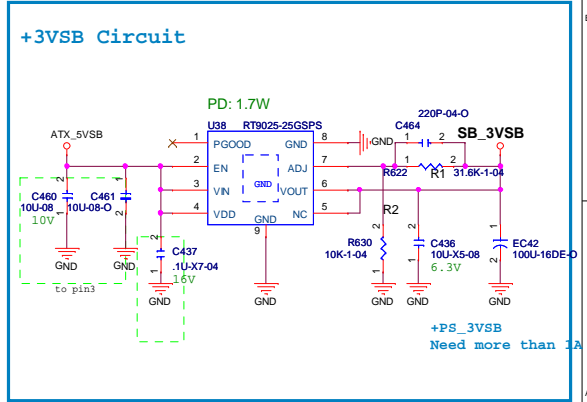
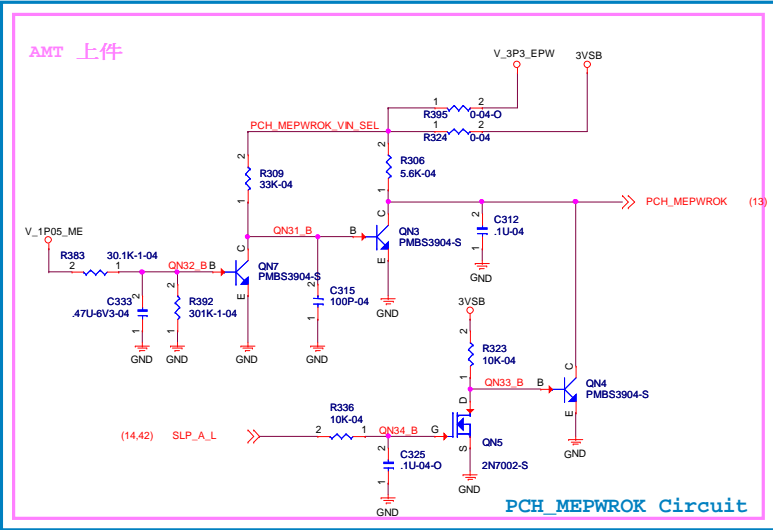
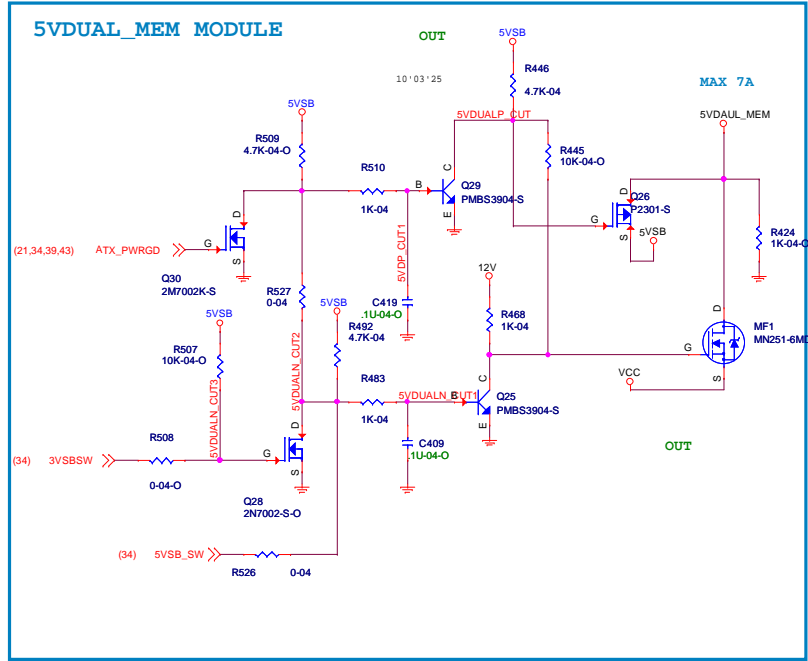
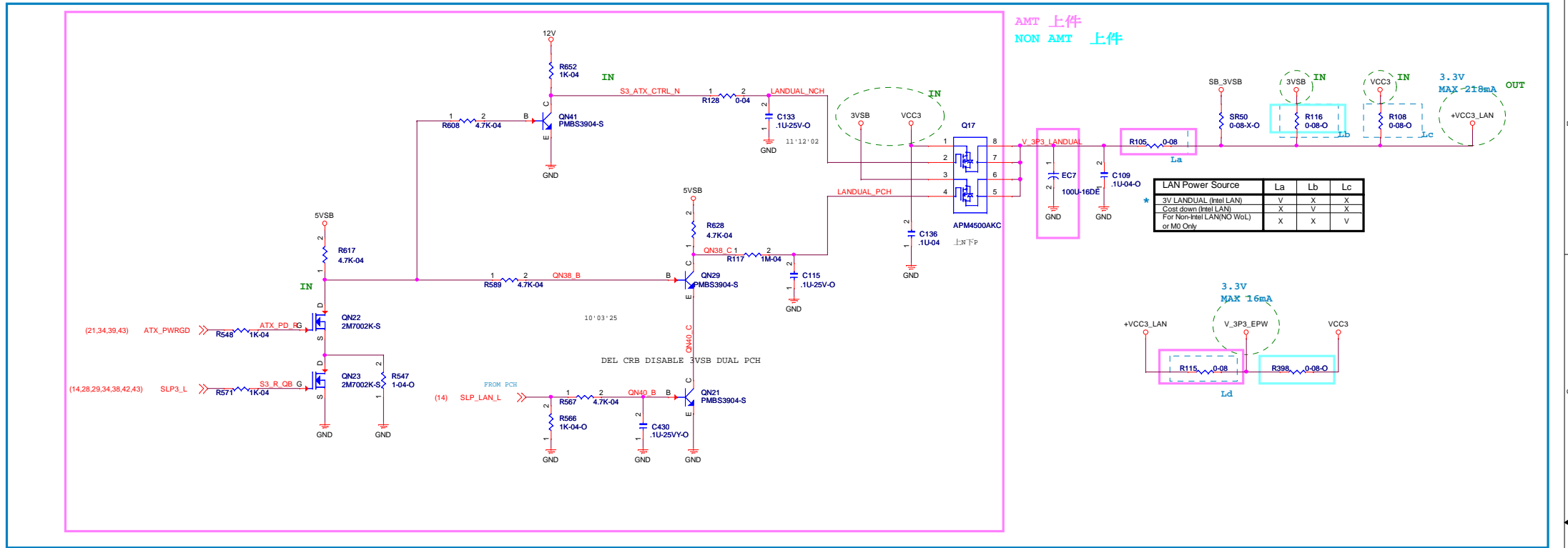
1

DPWROK\_5



## SUS\_QCR

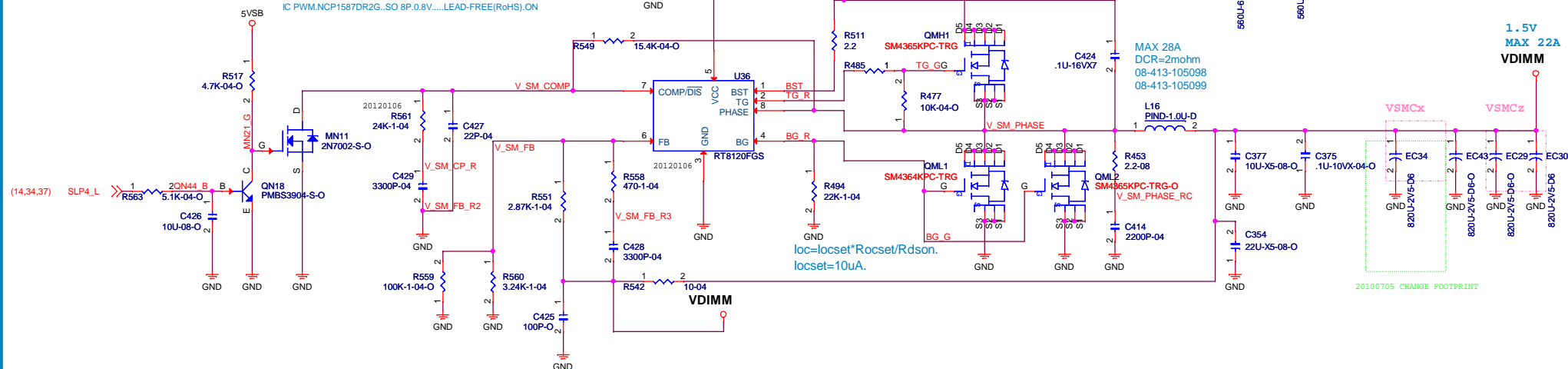




## VDIMM

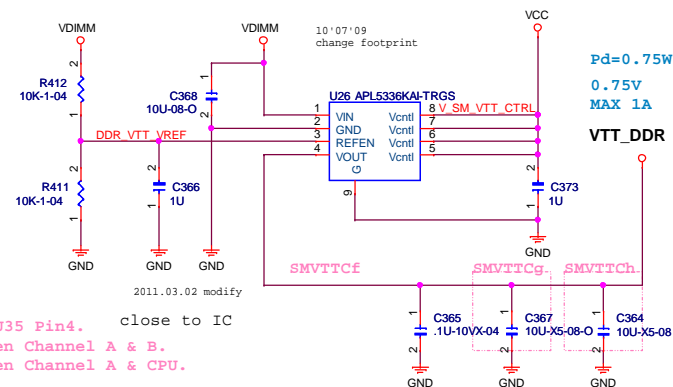
SLP4_L	High	Low
NCP1587DR2G	Enable	Disable

NCP1587 & RT8116 pin to pin.  
RT8116: boot voltage 30V.  
02-436-587890  
IC PWM.NCP1587DR2G..SO 8P.0.8V.....LEAD-FREE(RoHS).ON



## DDR\_VTT

AP5336/GS9020/AME9172M



Elitegroup Computer Systems

Title	DC/DC VDIMM/DDR_VTT		
Size	Document Number	Rev	
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VCCIO voltage selection	
VTT_SEL	CPU_VTT
low	1V
high	1.05V



- $I_{SS}$  is the soft-start current source at the 20 $\mu$ A limit
- $V_{SREF}$  is the buffered  $V_{REF}$  reference voltage

Frequency selection	
F (Hz)	FSEL
300K	Directly to GND
500K	Floating
600K	100K ohm to GND
1M	Pull-up to VCC

TABLE 2. ISL95870B VID TRUTH TABLE

VID STATE		RESULT		
VID1	VID0	CLOSE	V <sub>SREF</sub>	V <sub>OUT</sub>
1	1	SW0	V <sub>SET1</sub>	V <sub>OUT1</sub>
1	0	SW1	V <sub>SET2</sub>	V <sub>OUT2</sub>
0	1	SW2	V <sub>SET3</sub>	V <sub>OUT3</sub>
0	0	SW3	V <sub>SET4</sub>	V <sub>OUT4</sub>

The ISL95870B  $V_{SET1}$  setpoint is written as Equation 21:

$$V_{SET1} = V_{REF} \quad (\text{EQ. 21})$$

The ISL95870B  $V_{SET2}$  setpoint is written as Equation 22:

$$V_{SET2} = V_{REF} \cdot \left( 1 + \frac{R_{SET1}}{R_{SET2} + R_{SET3} + R_{SET4}} \right) \quad (\text{EQ. 22})$$

The ISL95870B  $V_{SET3}$  setpoint is written as Equation 23:

$$V_{SET3} = V_{REF} \cdot \left( 1 + \frac{R_{SET1} + R_{SET2}}{R_{SET3} + R_{SET4}} \right) \quad (\text{EQ. 23})$$

The ISL95870B  $V_{SET4}$  setpoint is written as Equation 24:

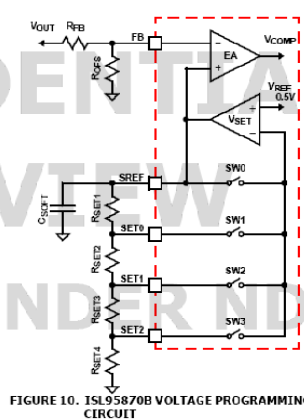
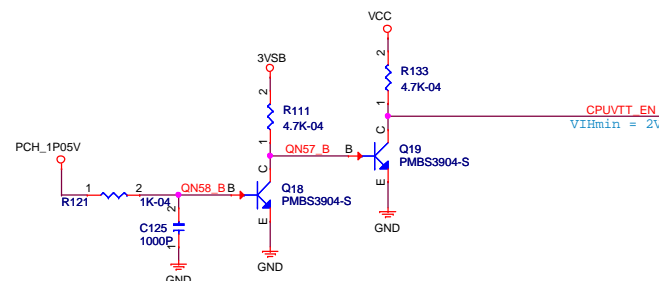
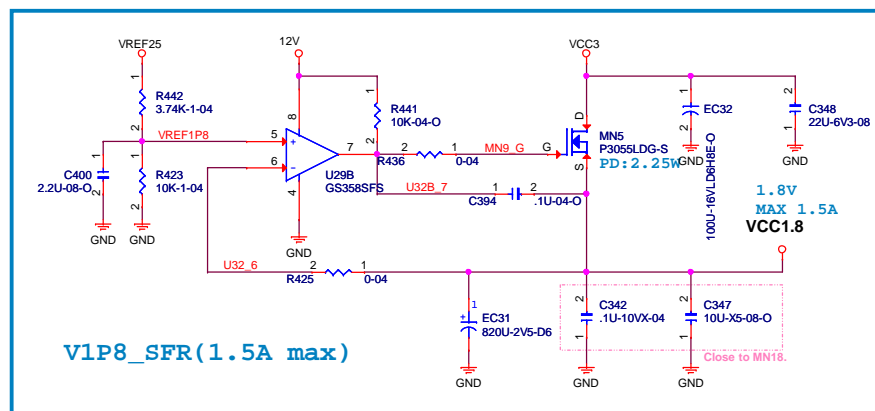
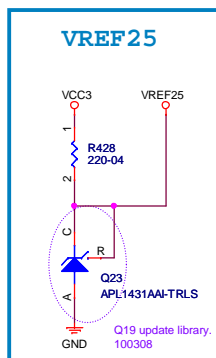
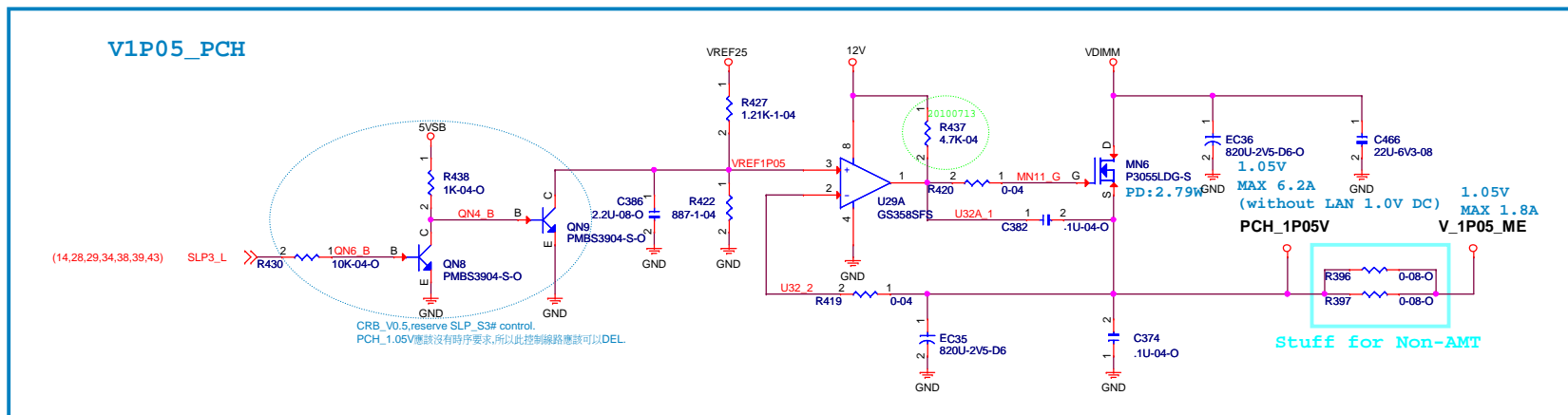
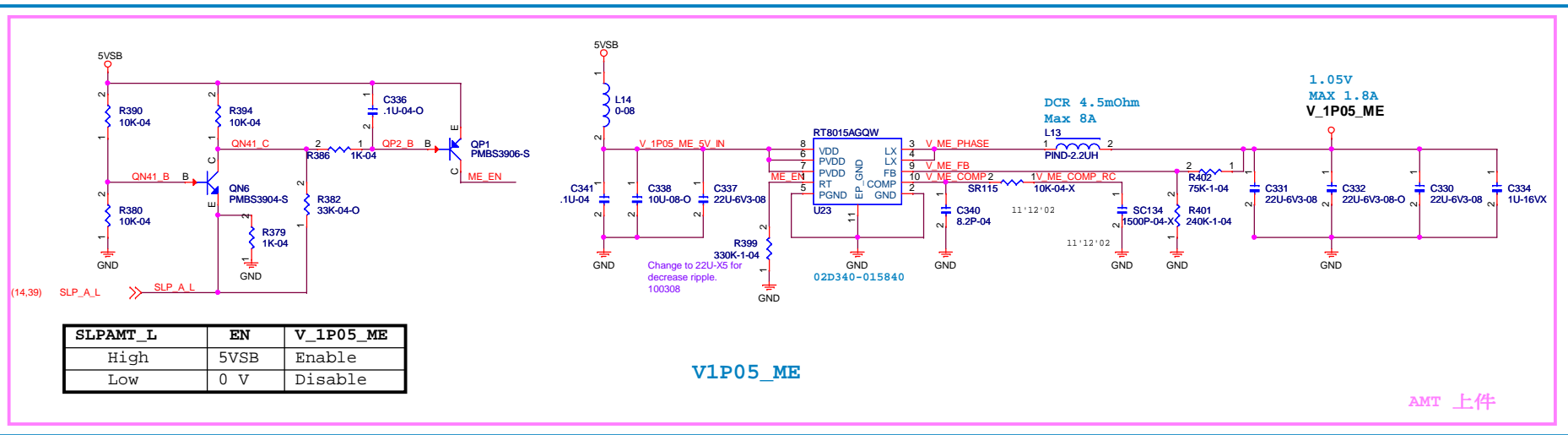
$$V_{SET4} = V_{REF} \cdot \left( 1 + \frac{R_{SET1} + R_{SET2} + R_{SET3}}{R_{SET4}} \right) \quad (EQ. 24)$$


FIGURE 10. ISL95870B VOLTAGE PROGRAMMING CIRCUIT





Stuff VSAGz

VCCSA voltage selection	
VID	+V_SA
0	0.925V
1	0.85V

\*

VCCSA voltage selection	
VID	+V <sub>SA</sub>
0	0.925V
1	0.85V

\*

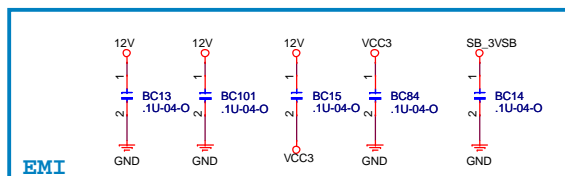
VCCSA voltage selection	
Rf	+V_SA
unstuffed	0.85V
stuffed	0.925V

VCCSA voltage selection	
Rf	+V_SA
unstuffed	0.85V
stuffed	0.925V



OUTPUT	Minimum Current (A)
+12V V1DC1	0.1
+12V V1DC2	0.5 (CPU)
+5 VDC	0.2
+3.3 VDC	0.1
-12 VDC	0
+5 VSB	0

OUTPUT	Minimum Current (A)
+12V V1DC1	0.1
+12V V1DC2	0.5(CPU)
+5 VDC	0.2
+3.3 VDC	0.1
-12 VDC	0
+5 VSB	0



**VCCSA Sequence**

(41) VTT\_PWRGD

R466 0-04-O

5VSB

R521 10K-04

QN5 B

QN10 PMBS3904-S

Q

B

GND

QN13 PMBS3904-S

Q

B

GND

R484 10K-04

QN3 B

2

1

(14,28,29,34,38,39,42) SLP3\_L

R523 10K-04

QN8 B

2

1

5VSB

R522 10K-04

QN7 B

QN11 PMBS3904-S

Q

B

GND

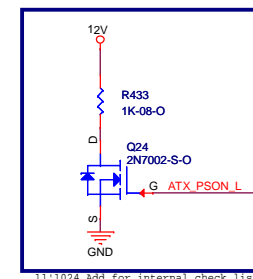
QN14 PMBS3904-S

Q

B

GND

VCCSA\_COMP





(38) VR\_EN  
(5) VR\_SVID\_ALERT\_L  
(5) VR\_SVID\_DATAOUT  
(5) VR\_SVID\_CLK

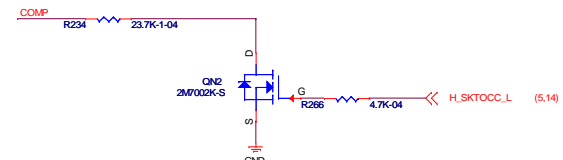
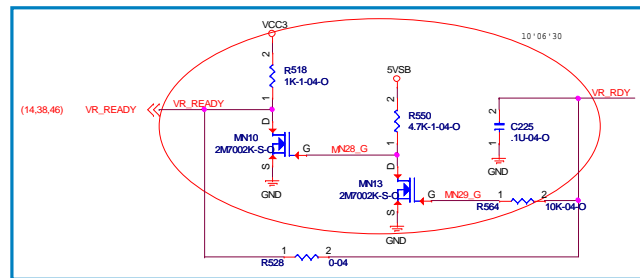
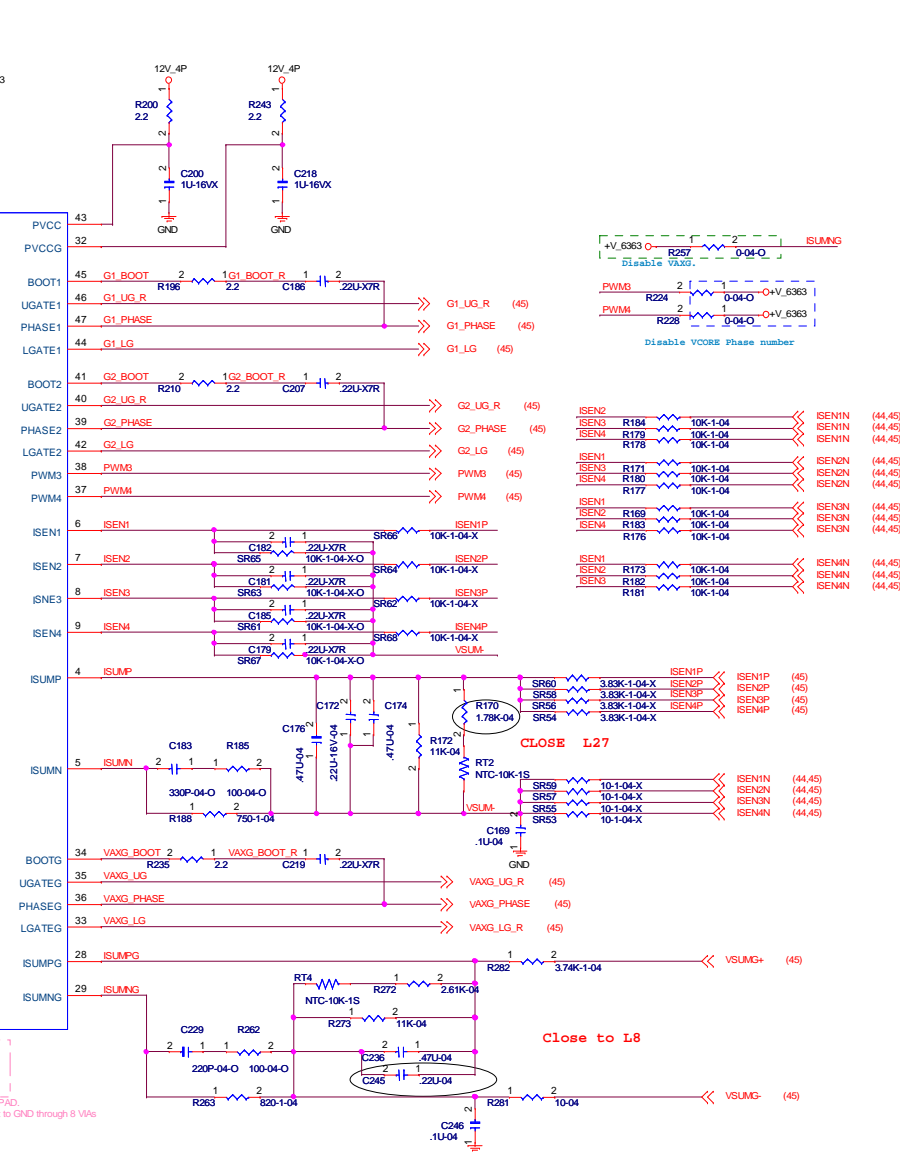
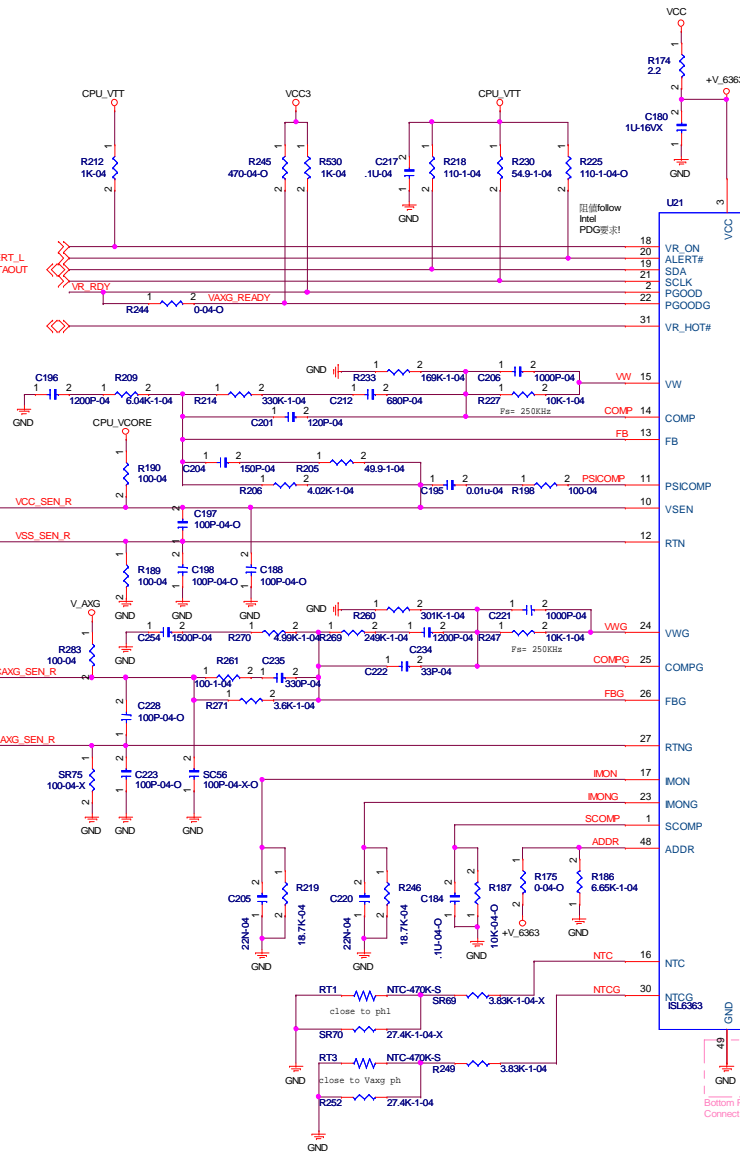
(5) VR\_HOT\_L

(5) VCC\_SEN

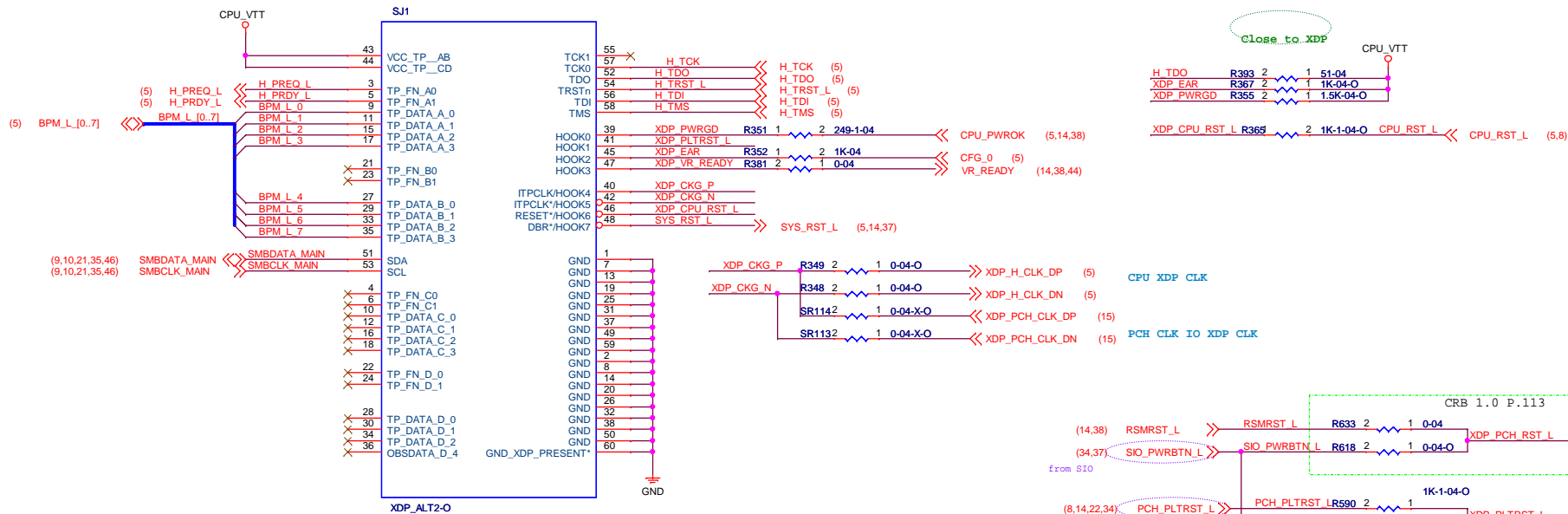
(5) VSS\_SEN

(5) VCCAVX\_SEN

(5) VSSAVX\_SEN



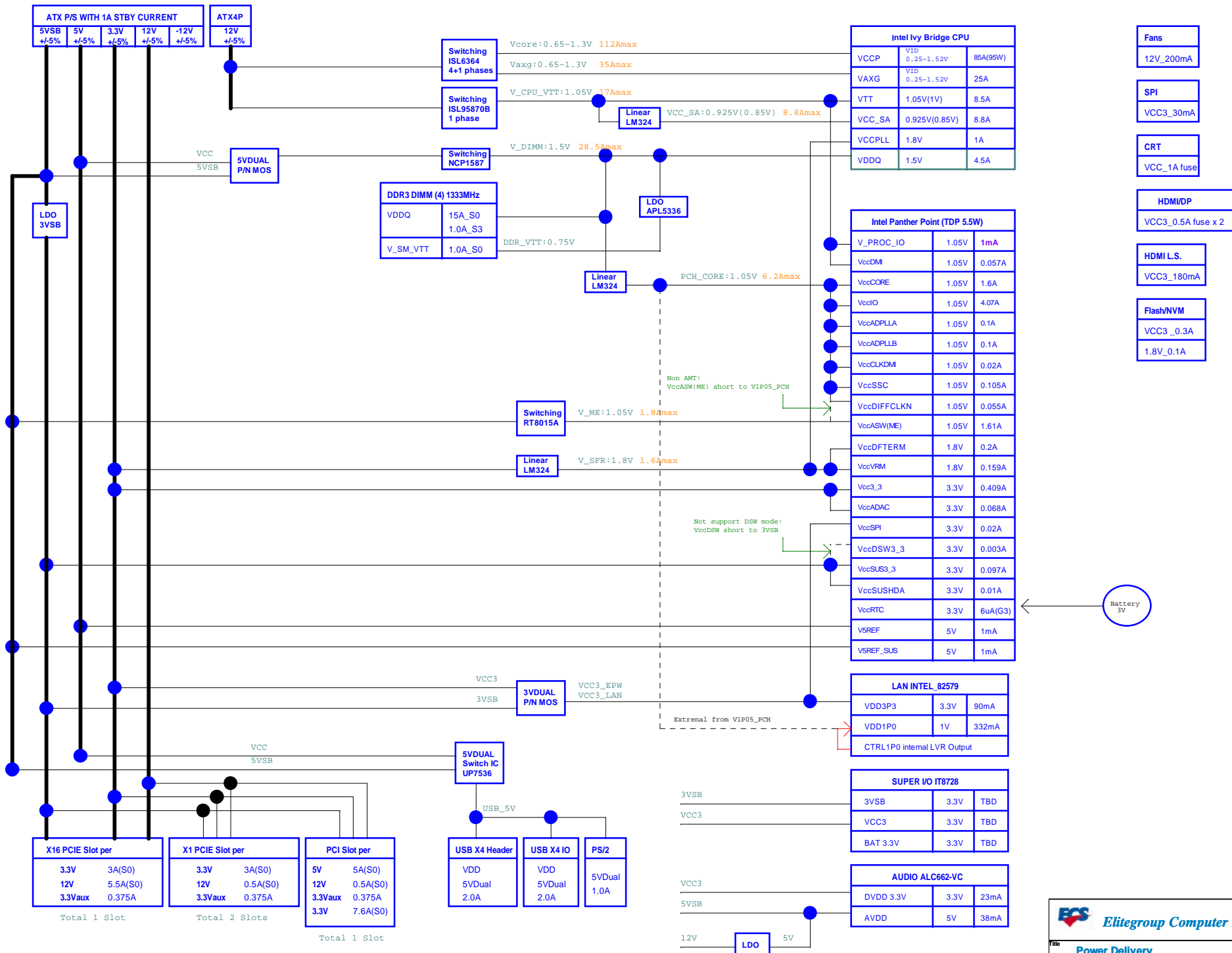




DESIGN NOTE:  
PCH JTAG

DESIGN NOTE:  
DEFENSIVE DESIGN

Title <b>XDP</b>		
Size Custom	Document Number <b>Q77H2-AD</b>	Rev <b>1.0</b>
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Fans
12V_200mA

SPI
VCC3_30mA

CRT
VCC_1A fuse

HDMI/DP
VCC3_0.5A fuse x 2

HDMI L.S.
VCC3_180mA

Flash/NVM
VCC3_0.3A
1.8V_0.1A

